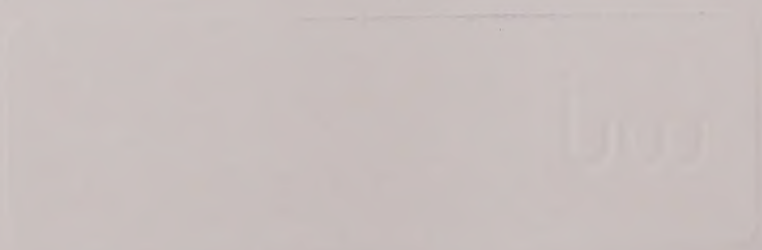


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INSTRUCTION MANUAL
FOR
WJ-9518BE-9S FDM DEMODULATOR



WATKINS-JOHNSON



INSTRUCTION MANUAL
FOR
WJ-9518BE-9S FDM DEMODULATOR

WATKINS-JOHNSON COMPANY
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Gaithersburg, Maryland 20878

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PROPRIETARY STATEMENT

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WARNING

This equipment utilizes voltages which are potentially dangerous and may be fatal if contacted. Exercise extreme caution when working on the equipment with any protective cover removed.

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GENERAL DESCRIPTION

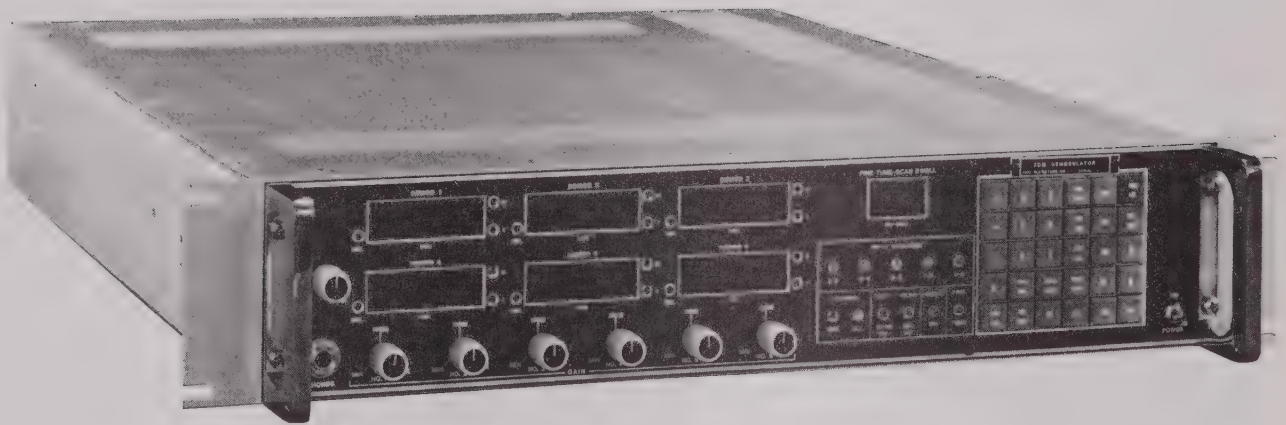


Figure 1-1. WJ-9518BE-9S FDM Demodulator

SECTION I

GENERAL DESCRIPTION

1.1 ELECTRICAL CHARACTERISTICS

The WJ-9518BE-9S FDM Demodulator has a tuning range from 0-15 MHz. It receives and demodulates baseband frequencies from 300 Hz to 15 MHz. Six independent demodulator channels, contained within the WJ-9518BE-9S, demodulate the received baseband signals in either the Upright or Inverted mode. Demodulator channel inputs can be either independent, providing demodulation for six different baseband inputs, or bridged, combining two or all of the demodulator channels to process the same input signal. Demodulated baseband signals provide a 300-3850 Hz audio signal to six independent rear panel connectors. Refer to **Table 1-1** for a list of specifications.

Control of the selected demodulator operating parameters, other than the head-phone level and the demodulator gains, are accomplished via the front panel keyboard. The keyboard selects the demodulator (1-6) that is under active control. Controlling one demodulator channel at a time, the keyboard selects: the demodulator channel frequency, bridging, start and stop frequencies, dwell time, step size, and the mode of operation (Upright or Inverted). Selection of the demodulator channel tuned frequency is accomplished either directly or indirectly via the keyboard. Direct frequency selection is accomplished by entering the desired frequency, in kHz, via the keyboard. Indirect frequency selection is accomplished via entering the CCITT Standard for the 2700 or 960 channel plan. The normal 1 kHz tuning resolution can be varied an additional ± 50 Hz, in 5 Hz steps, via depressing the FINE TUNE pushbutton and then utilizing the increment ($\uparrow$) or decrement ($\downarrow$) pushbuttons to vary the tuning. In addition to fixed frequency operation, the demodulator channels are able to scan between two preset frequencies (F1 and F2), with a selectable frequency step (1 kHz to 1 MHz) and a selectable dwell time (0.2 to 9.9 seconds).

1.2 MECHANICAL CHARACTERISTICS

The WJ-9518BE-9S Demodulator is designed to be mounted into a standard 19-inch equipment rack frame. The demodulator is 19 inches wide, occupies 3.5 inches of vertical space and extends 20.75 inches into the rack. Construction of the main chassis, internal partitions, top cover, rear panel and front panel are of aluminum. Mounted on the front panel is a black anodized aluminum bezel with etched display and control markings. Mounted through the front panel are all the controls (POWER, GAIN, Phone level and the 30 pushbutton keypad) and the indicators (single and 8 segment LEDs) necessary for energizing and controlling the unit operation. Except for the headphone jack on the front panel, all input and output connectors are located on the rear panel. Voltage selector switch S2, located on the rear panel allows selection of either 115 or 230 Vac line voltage operation.

Loosening the top cover's quarter-turn fasteners, which secure the cover to the main chassis, permit the internal subassemblies to be accessed when the cover is removed.

1.3

EQUIPMENT SUPPLIED

The equipment supplied consists of:

- 1) One WJ-9518BE-9S Demodulator Unit
- 2) One Detachable Line Power Cord
- 3) Three Extender Cards.

1.4

EQUIPMENT REQUIRED BUT NOT SUPPLIED

To obtain maximum demodulator capabilities, equipment from the following list should be selected.

- 1) Audio monitoring equipment
600 ohm headphone set or
600 ohm speaker panel
- 2) HP-85 calculator (with IEEE-488 option) for remote control operation.

Table 1-1. WJ-9518BE-9S FDM Demodulator, Specifications

Input Impedance	75 Ω , unbalanced
Input Tuning Range	0 to 15 MHz
Input Frequency Range	300 Hz to 15 MHz
Number of Inputs	Six, baseband
Input Level	-25 dBm, nominal, single tone
Operation Mode	Single sideband, Upright or Inverted
Unit Control	Local - via the front panel controls Remote - via the IEEE-488 BUS
Adjacent Channel Rejection	45 dB, minimum, at 300 Hz and 3700 Hz
Demodulator Crosstalk	57 dB, minimum
Noise Power Ratio	44 dB, minimum with an input noise level of -7 dBm and a 2.5 MHz noise BW
Residual Noise	57 dB, minimum, below the nominal output level (12 kHz - 15 MHz)
Tuning Scheme	CCITT Plan (960 or 2700 Channel) or Direct
Tuning Resolution	
Normal	4 kHz (for CCITT Plan) or 1 kHz (for Direct)
Fine	± 50 Hz, in 5 Hz steps
Number of Outputs	Six, audio
Output Impedance	600 Ω , unbalanced
Output Frequency	300 Hz to 3850 Hz, minimum, at the 3 dB points
Output Level	1 V rms ± 0.1 V, into 600 ohms
Bandpass Ripple	1.5 dB maximum
Spurious Outputs	50 dB, minimum, below nominal output level with a -25 dBm input test tone signal
Group Delay	400-3550 Hz, 200 μ sec, maximum 300-3650 Hz, 500 μ sec, maximum 200-3750 Hz, 1000 μ sec, maximum

Table 1-1. WJ-9518BE-9 FDM Demodulator, Specifications (Cont'd)

Reference Frequency	
Internal	1 MHz
External	1 MHz
Reference Frequency Accuracy	$\pm 1 \times 10^{-6}$ Hz per year, internally adjusted
Reference Frequency Stability	$\pm 1 \times 10^{-6}$ Hz per day, after a 30 minute warm-up
Headphone Output Level	10 mW, minimum, into a 600 ohm load
Operational Temperature Range	0°C to 50°C
Specification Compliance Range	15°C to 35°C
Input Voltage Requirement	115/230 Vac, $\pm 10\%$, 50 Hz to 60 Hz
Power Consumption	45 Watts, approximately
Dimensions	
Depth	22.0 inches (56 cm)
Width	19.0 inches (48 cm)
Height	3.5 inches (8.9 cm)
Weight	40 lbs. (21 kg) approximately

SECTION II
INSTALLATION AND OPERATION

SECTION II

INSTALLATION AND OPERATION

2.1 UNPACKING AND INSPECTION

Upon receipt of the shipment, examine the shipping container for any visible signs of damage before unpacking the equipment. If the shipping container is visibly damaged, attempt to have the carrier's agent present when the equipment is unpacked. If the carrier's agent cannot be present while unpacking the equipment and equipment damage is discovered, retain all packing materials and the shipping container for the carrier's inspection. Also, verify that the received equipment is complete as listed on the packing slip. If any discrepancies or shortages are discovered, contact the Watkins-Johnson Company, Special Projects Division, or your Watkins-Johnson representative.

2.2 INSTALLATION

This demodulator is designed for mounting into a standard 19-inch equipment rack. The unit extends 20.75 inches into the equipment rack frame and occupies 3.5 inches of vertical space. When rack mounting the WJ-9518BE-9S, do not rely entirely on the front panel mountings to support the unit weight. The use of slides, mounted to the sides of the unit is recommended. Acceptance mounting holes for Jonathan Type QD 110 slides, or an equivalent slide, are already provided. The rack environment should allow for a free flow of air through the top dust cover and around the outer surfaces of the demodulator. A 1.75 inch free-air space above and below the unit is recommended for a rack mount environment, along with forced air convection.

NOTE

Prior to installing the WJ-9518BE-9S in its final location, ensure line voltage selector switch S1 is set for the proper line voltage operation (115 or 230 Vac).

Access to the rear panel should be provided to allow changes in cable connections to be conveniently performed, if desired. These rear panel cable connections and the front panel connection are described in **Table 2-1**. Refer to **Figure 2-1** to view the rear panel connector locations.

2.2.1 **CONNECTOR SIGNALS**

2.2.1.1 Line Voltage Receptacle FL1J1 — This three prong, male, connector receptacle mates with the power cord to apply line voltage to the demodulator through the internal line filter.

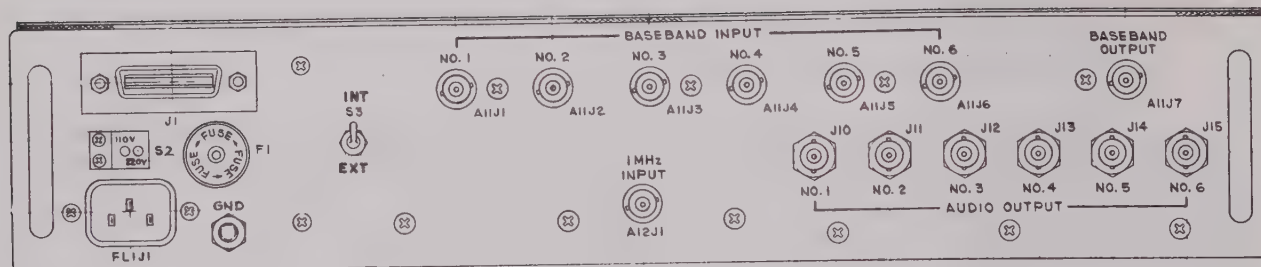


Figure 2-1. Rear Panel View

2.2.1.2 **IEEE-488 Connector J1** — This multipin connector provides the ability to be controlled remotely via a suitable remote controller.

2.2.1.3 **Baseband Input A11J1 - A11J6** — These six BNC type connectors apply the received -25 dBm baseband frequencies (300 Hz - 15 MHz) to the demodulator channels.

2.2.1.4 **Baseband Output A11J7** — This BNC type connector provides a sample of the 300 Hz - 15 MHz baseband output signal at a -25 dBm level, into a 75 ohm load.

2.2.1.5 **1 MHz Input A12J1** — This BNC type connector receives external 1 MHz reference signals, with a typical input level of 0 dBm, when switch S3 is in the EXT position.

2.2.1.6 **Audio Output J10 - J15** — These six BNC type connectors provide a 600 ohm demodulated audio output (300 Hz - 3850 Hz) at a 1 V rms level from each demodulator channel.

Table 2-1. Table of Connectors

Connector	Type	Purpose
PHONES	Phone Jack Recptacle (600 ohm)	Provides an audio output for the selected demodulator.
J1	IEEE-488 Multipin BUS	Allows control via a suitable remote controller.

Table 2-1. Table of Connectors (Cont'd)

Connector	Type	Purpose
FL1J1	3 Prong Male Receptacle	Provides the connection for line power.
A11J2 Thru A11J6	BNC Type Female Connector (75 ohm)	Accepts BASEBAND INPUT signals for demodulation.
A11J7	BNC Type Female Connector (75 ohm)	Provides a sample BASEBAND OUTPUT signal.
A12J1	BNC Type Female Connector (50 ohm)	Accepts an external 1 MHz INPUT reference signal.
J10 Thru J15	BNC Type Female Connector (600 ohm)	Provide an audio output from each demodulator.

2.3**EQUIPMENT MALFUNCTIONS**

This unit was thoroughly inspected and factory adjusted for optimum performance prior to shipment. If an apparent malfunction is encountered after performing the recommended installation procedures, verify that the correct input signals are present at the proper jacks. Maintenance and troubleshooting of this unit may be aided by the procedures described in **Section IV** of this manual. Prior to taking any corrective maintenance action or breaking any seals, contact your Watkins-Johnson representative or the Watkins-Johnson Company, Special Projects Division, Gaithersburg, Maryland to prevent the possibility of voiding the terms of warranty.

2.4**OPERATION**

The WJ-9518BE-9S FDM Demodulator is capable of either local or remote control. During the local mode of operation, unit operating parameters are varied by use of the front panel controls described in **paragraph 2.4.1** and listed in **Table 2-2**. The demodulator under front panel control is indicated via the illuminated SEL LED. Pressing the REM/LCL pushbutton toggles unit control from local to remote control and is indicated via the front panel REM or LCL illuminated LED. Remote control is accomplished via a suitable controller connected to the IEEE-488 Standard connector (J1). **Figure 2-2** illustrates the front panel of controls and typical display information.

2.4.1**CONTROLS AND INDICATORS****2.4.1.1**

POWER ON – This single pole, double throw toggle switch applies the line voltage to the unit when in the up (ON) position. In the down position, line voltage to the unit is interrupted.

On power up, the operating parameters are set to the same parameter settings that had been active at the time line voltage to the unit was interrupted. If the battery back-up memory is lost, the unit on power up is initialized to the following parameter settings:

Demodulator Select	Demod 1
Frequency	0 kHz
Mode	U (upright)
Fine Tuning	0 Hz
Scan Dwell	0.1 sec
Input Bridging	Off
Control	Local
Scan	Off
Fine Tune	Off
CCITT PLAN	Off

NOTE

At power up, a five minute delay is required to allow the Reference Generator TCXO to stabilize. When switching the reference from EXT to INT, allow two minutes for the frequency to stabilize.

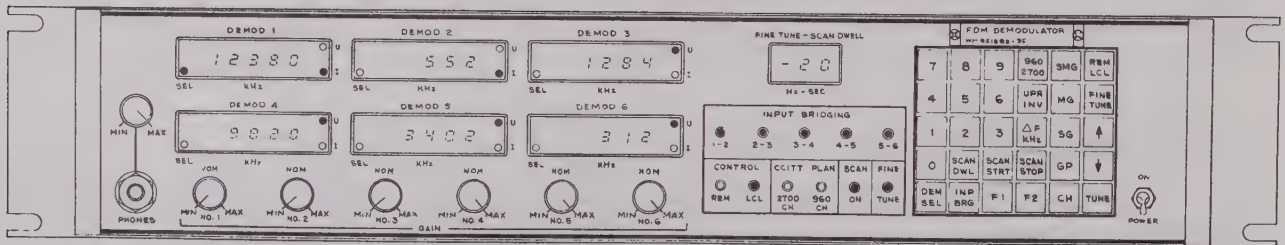


Figure 2-2. Front Panel View

2.4.1.2 PHONES (MIN/MAX) – This control knob varies the 600 ohm audio output level at the front panel phone jack for the selected demodulator. The control knob audio control range is approximately 40 dB.

2.4.1.3 **GAIN (No. 1 - No. 6)** – These six control knobs are utilized to control the gain of the corresponding demodulator. The demodulator gain control range is approximately 10 dB. During remote operation, the gain control knobs are disabled.

2.4.1.4 **DEMODO (1-6)** – These six multiple LED displays provide the demodulator tuned frequency, the mode selected: Upright (UPR) or Inverted (INV) and the selected demodulator (SEL). Frequency is displayed in kHz for direct tuning or in channels for the CCITT Plan via the six 7-segment LEDs. The mode and selected demodulator are indicated via illuminating a single LED.

2.4.1.5 **FINE TUNE - SCAN DWELL** – This three element, 7-segment LED display indicates the Fine Tuning offset in Hertz (± 50 Hz in 5 Hz steps) for all six demodulators. Negative Fine Tune frequencies are preceded by a minus sign (-). Scan Dwell is displayed in the same indicator space as the Fine Tune. Scan Dwell time (0.2 - 9.9 seconds in 0.1 sec. steps) is preceded by a **d**, indicating that Dwell is selected, represents the time between frequency steps.

2.4.1.6 **INPUT BRIDGING** – This five LED display, visually indicates when input bridging exists between adjacent demodulators. When the LED is illuminated, input bridging exists between the associated demodulators whose numbers appear below the lit LED. Bridging is cleared via pressing the 0 key.

2.4.1.7 **CONTROL** – These two LEDs indicate whether the unit is under remote (REM) or local (LCL) control. The illuminated LED indicates which mode of control is selected.

2.4.1.8 **CCITT PLAN** – When either of these two LEDs is illuminated, the CCITT Standard is selected (either the 2700 channel plan or the 960 channel plan) for tuning the frequency of the selected demodulator.

2.4.1.9 **SCAN ON** – Illumination of this LED indicates that the selected demodulator is scanning between the preset start (F1) and stop (F2) frequencies.

2.4.1.10 **FINE TUNE** – This LED illuminates when a FINE TUNE frequency, other than 0, has been selected. Only the increment or decrement keys can be utilized to vary the FINE TUNE frequency. Pressing any other key disables FINE TUNE.

2.4.1.11 **Numerical Pushbuttons (0-9)** – These ten pushbuttons are utilized for: demodulator selection, frequency selection, CCITT Standard channel selection, dwell time, input bridging, start and stop frequencies.

2.4.1.12 **960/2700** – Depressing this pushbutton selects the CCITT Standard for the 960 or 2700 channel system or the direct frequency mode for the selected demodulator's frequency. Cycling through the direct frequency and back to either CCITT mode causes all zeros to be displayed for the selected CCITT mode.

2.4.1.13 **SMG** – Depressing this pushbutton enables the numerical keys to select the CCITT Supermastergroup (1-3) for the 2700 channel plan.

2.4.1.14 **MG** – Depressing this pushbutton enables the numerical keys to select the desired CCITT Standard Mastergroup (7-9) for the 2700 channel plan.

2.4.1.15 **SG** – Depressing this pushbutton allows selection of the CCITT Standard Supergroup. Supergroups 1-16 may be selected for the 960 channel plan or Supergroups 4-8 for the 2700 channel plan.

2.4.1.16 **GP** – Depressing this key enables the numerical keys to select the CCITT Standard Group. Groups 1-5 may be selected for both the 2700 and 960 channel plans.

2.4.1.17 **CH** – Depressing this pushbutton enables the numerical keys to select the CCITT Standard Channel (1-12) for both the 960 and 2700 channel plans.

2.4.1.18 **REM/LCL** – This dual function pushbutton toggles unit control from one control state to the other, indicating whether the unit is in the local (LCL) or remote (REM) control mode.

2.4.1.19 **UPR/INV** – Depressing this dual function pushbutton alternately selects the Upright or Inverted mode of detection for the demodulator under front panel control. (Not selectable for CCITT Plan.)

2.4.1.20 **FINE TUNE** – When this pushbutton is initially pressed, the FINE TUNE LED illuminates, the FINE TUNE - SCAN DWELL indicator displays the fine tuning offset, and the increment () and decrement () keys step the FINE TUNE frequency in 5 Hz steps.

2.4.1.21 – Depressing this increment pushbutton after depressing FINE TUNE causes the displayed Fine Tune frequency to increase by 5 Hz, up to 50 Hz above the displayed demodulator frequency. After depressing TUNE, holding the increment key depressed causes the displayed frequency to make 3 steps at the normal rate and then the step rate becomes 3 times the normal rate. Depressing the increment key, without previously depressing any other pushbutton, increments the selected demodulator.

2.4.1.22 – The decrement key, when depressed after the FINE TUNE key was pressed, decreases the displayed fine tune frequency by 5 Hz each time the key is depressed until the fine tune frequency is -50 Hz. Holding the decrement key depressed causes the frequency to step 3 times at a normal rate and then step at 3 times the normal step rate. Only depressing the decrement key decreases the selected demodulator.

2.4.1.23 **SCAN DWL** – This pushbutton, when pressed, allows the numerical keys to select the scan dwell time from 0.2 to 9.9 seconds in 0.1 second steps.

2.4.1.24 **F1** – This key is depressed after entering the desired start frequency (kHz or CCITT Standard).

2.4.1.25 **F2** – This key is depressed after entering the desired stop frequency (kHz or CCITT Standard).

2.4.1.26 **ΔF kHz** – This pushbutton is depressed to enable the numerical keys to select the size of the frequency step for the Scan mode. The size of ΔF is from 1 to 1000 kHz in 1 kHz steps. (ΔF is NOT selectable for either CCITT Plan.)

2.4.1.27 **SCAN STRT** – Depressing this pushbutton causes the selected demodulator to start scanning. The step size (ΔF kHz), dwell time (SCAN DWL), start frequency (F1) and stop frequency (F2) must be set prior to starting the Scan mode of operation. (ΔF kHz is set to 4 kHz for both CCITT Plans.) If $F1 > F2$ the frequency scans down. If $F1 < F2$ the frequency scans up.

2.4.1.28 **SCAN STOP** – Depressing this pushbutton stops the frequency scan at the displayed frequency or channel, depending on the selected frequency mode of operation.

2.4.1.29 **DEM SEL** – Depressing this pushbutton enables the numerical keys (1-6) to select one of the six demodulators for control by the front panel. It can also be depressed to clear any unfinished command.

2.4.1.30 **INP BRG** – Depressing this pushbutton enables the numerical keys (1-6) to select bridging of the input baseband signal to more than one demodulator. Depressing two adjacent demodulator numerical keys causes the bridging between the two adjacent demodulators to change states. If the selected bridging numbers are not adjacent, then input bridging occurs from the first number through the second demodulator number and illuminates the LEDs of the bridged demodulators. When input bridging is selected, the INPUT BRIDGING LED illuminates to indicate which demodulators are bridged. Entering a 0 unbridges all demodulators.

2.4.1.31 **TUNE** – Depressing this pushbutton enters the selected CCITT Standard and tunes the selected demodulator to the designated frequency for the CCITT selection. Depressing this key clears any unfinished nonnumerical command. The demodulator tuned frequency can manually be stepped by depressing the TUNE key and then pressing the increment or decrement key. When either CCITT Plan is selected, holding the TUNE in displays the direct frequency for the selected CCITT channel.

2.4.1.32 **S2 LINE SELECT** – This rear panel toggle switch is set to the left for 115 V or to the right for 230 V. To change the selected line voltage, remove the two crosshead screws securing the plate that S2 extends through and move the switch. Insert the switch handle through the hole in the metal plate and secure the plate to the rear panel via the two screws.

2.4.1.33 S3 INT/EXT — This rear panel toggle switch selects the reference source to be used by the Reference Generator. In the INT position (switch up) the reference is from the internal TCXO. In the EXT position (switch down) an external 1 MHz reference signal must be connected to A12J1. When switching from an external reference (EXT) to the internal reference (INT), allow two minutes for the frequency to stabilize.

Table 2-2. Controls and Indicators

PHONES (MIN/MAX)	Controls the headphone output level for the demodulator under front panel control.
SEL	Single LED illuminates to indicate which demodulator is selected for front panel control.
DEMODO (1-6)	Six 7-segment LEDs to display the demodulator's tuned frequency.
U	Single LED illuminates when the Upright detection mode is selected.
I	Single LED illuminates when the Inverted detection mode is selected.
GAIN (No. 1 - No. 6)	A control knob to vary the gain of each demodulator.
FINE TUNE - SCAN DWELL	Three 7-segment LEDs which display the FINE TUNE offset, in 5 Hz steps. Displays the selected dwell time, in 0.1 second steps, when the display is preceeded by d .
INPUT BRIDGING	Five single LEDs which illuminate to indicate when bridging is selected between demodulators.
CONTROL (REM/LCL)	Two single LEDs indicate whether the unit is under remote or local control.
CCITT PLAN	Two single LEDs indicate which CCITT Plan (960 or 2700 channels) is selected.
SCAN (ON)	This single LED illuminates when the selected demodulator is scanning.
FINE TUNE	A single LED that illuminates when the fine tune frequency is other than 0 Hz.
KEYPAD	
0 thru 9	Numerical keys used to select the demodulator, frequency, bridging, dwell, step size, start and stop frequencies.
*960/2700	Selects the frequency tuning mode selected demodulator. Selects 960, 2700 or direct tuning plan.
SMG	Enables the numerical keys to select the Super-mastergroup (1-3) for the 2700 CCITT Plan.
REM/LCL	Toggles the unit between local and remote operation.
*UPR/INV	Selects the Upright or Inverted mode of operation for the selected demodulator, when direct tuning is selected.
MG	Enables the numerical keys to select the Master-group (7-9) for the 2700 CCITT Plan.

* Multifunction Operation Key

Table 2-2. Controls and Indicators (Cont'd)

FINE TUNE	Enables the increment (↑) and decrement (↓) keys to control the fine tuning offset frequency.
ΔF kHz	Enables the numerical keys to select the frequency step size (1-1000 kHz).
SG	Enables the numerical keys to select the Super-group for the CCITT Plan (1-16 for 960 or 4-8 for 2700 Plan).
↑	Increments parameters that can be controlled.
SCAN DWL	Enables the numerical keys to select the dwell time for scan operation.
SCAN START	Starts the selected demodulator scanning after the step size, dwell, start and stop frequencies have been determined.
SCAN STOP	Stops the scanning of the selected demodulator.
GP	Enables the numerical keys to select the Group (1-5) for the CCITT Plan.
↓	Decreases controllable front panel parameters.
DEM SEL	Enables the numerical keys to select the demodulator for front panel control. Also clears undesired numerical entries.
INP BRG	Enables the numerical keys to select which base-band input is shared between demodulators.
F1	Bridging is cleared by entering 0.
F2	Enables the numerical keys to select the frequency (start) for the scan mode to start from.
CH	Enables an end frequency (stop) to be selected via the numerical keys.
*TUNE	Enables the numerical keys to select the channel (1-12) for the CCITT Plan.
S1	Enters the selected discrete or CCITT Plan frequency into the demodulator under front panel control. Also utilized to clear undesired parameter changes that are incomplete.
S3	Selects the line voltage, either 115 or 230 Vac, to be utilized by the unit.
POWER (ON)	Selects the reference, either internal (INT) or external (EXT) utilized by the unit.
	Applies line voltage to the unit when in the ON position.

* Multifunction Operation Key

2.4.2 LOCAL OPERATION

2.4.2.1 Local Control

In the local mode of operation, all the operating parameters can be controlled via the front panel controls. All of the operating parameters are selected through use of the controls listed in **paragraph 2.4.1**. **Table 2-3** lists the local control parameters and the sequence required for their selection.

Table 2-3. Local Control Operation

PARAMETER CONTROL	SELECTION SEQUENCE																		
DEMODO Selection	Press the DEM SEL key. Enter the desired demodulator number (1-6) via the numerical keys or via the increment or decrement key.																		
Tuned Frequency	Press the 960/2700 key until both of the LEDs for the CCITT Plans are extinguished. Press the UPR/INV key to select Upright or Invert mode.																		
Direct	Enter the desired tuned frequency (0-15000) via the numerical keys. Press the TUNE key to tune the demodulator to the displayed frequency.																		
CCITT Plan	Press the 960/2700 key to select the desired CCITT Plan. (The tuning plan is indicated via the illuminated LED.) Enter the SMG, MG, SG, GP, or CH for the selected plan.																		
	<table><tr><td>2700</td><td>Key</td><td>960</td></tr><tr><td>1-3</td><td>SMG</td><td>---</td></tr><tr><td>7-9</td><td>MG</td><td>---</td></tr><tr><td>4-8</td><td>SG</td><td>01-16</td></tr><tr><td>1-5</td><td>GP</td><td>1-5</td></tr><tr><td>01-12</td><td>CH</td><td>01-12</td></tr></table>	2700	Key	960	1-3	SMG	---	7-9	MG	---	4-8	SG	01-16	1-5	GP	1-5	01-12	CH	01-12
2700	Key	960																	
1-3	SMG	---																	
7-9	MG	---																	
4-8	SG	01-16																	
1-5	GP	1-5																	
01-12	CH	01-12																	
	Pressing the group or channel keys cause the decimal point to the right of the number(s) to be entered flashes until the required number of digits are entered. Table 2-4 illustrates typical displays for both CCITT Plans. Pressing the TUNE key tunes the demodulator to the displayed CCITT equivalent frequency.																		
Scanning																			
Manual Step	Press the 960/2700 key to select direct tuning (both LEDs for CCITT Plan extinguished). Enter the desired frequency via the numerical keys. Press TUNE to tune the demodulator to the entered frequency. Press the numerical keys to select the step size (1-1000 kHz). Press the ΔF kHz to enter the step size. Depress either the increment or decrement key to step the frequency up or down.																		
(Direct Only)																			

Table 2-3. Local Control Operation (Cont'd)

PARAMETER CONTROL	SELECTION SEQUENCE
SCAN (Direct Only)	Select the start frequency (in kHz) via the numerical keys. Press the F1 key to enter the start frequency. Select the stop frequency (in kHz) via the numerical keys. Press the F2 key to enter the stop frequency. Select the desired step size via the numerical keys. Press ΔF kHz to enter the step size. Press the SCAN DWL key to select scan dwell. Enter the scan dwell via the numerical keys (0.2-9.9) or the increment or decrement key. Depress the SCAN START key to begin the scan. Depressing the SCAN STOP key halts the scan and displays the frequency where the scan stopped.
(CCITT Only)	Press the 960/2700 key to select one of the two CCITT Plan tuning schemes. Press the required CCITT Plan keys (SMG, MG, SG, GP and CH) to select the desired channel. Pressing the SCAN STRT key causes the scan to start. Scanning begins at the selected channel and continues up to channel 12 and then begins again at channel 1. Pressing the SMG, MG, SG, or GP key and then pressing the increment or decrement key allows the next selected group to scan channels 1-12.
Fine Tuning	Depress the FINE TUNE key to select Fine Tuning. Enter the fine tuning frequency via the increment or decrement key (± 50 Hz).
Input Bridging	Press the INP BRG key to select Input Bridging. Enter two digits (1-6) between which bridging is desired. Entering 0 clears all bridging.

2.4.2.2 Direct Tuning

This tuning scheme allows the desired tuned frequency to be selected by utilizing the numerical keys to enter the desired tuning frequency and depressing the TUNE key to tune the demodulator. The keyboard frequency is entered into the selected demodulator and is visible in the selected DEMOD display.

Selection of either the Upright or Inverted detection mode is varied via depressing the UPR/INV key, while in the direct tuning mode. This allows detection of the upper sideband (USB) or lower sideband (LSB) of a received baseband signal. A direct frequency may be stepped manually or swept automatically. Manual frequency step sizes are determined by the entered ΔF kHz. The demodulator tuned frequency is varied via the numerical keys or the increment or decrement key. Frequency step sizes (ΔF kHz) are selectable from 1-1000 kHz, in 1 kHz increments to vary the size of the frequency step.

Manual direct tuning provides the capability to select, via the keyboard, any frequency within the baseband range, 0-15 MHz in 1 kHz increments, in either the Upright (U) or Inverted (I) mode. Each demodulator is able to be individually controlled, via the DEM SEL key and numerical keys (1-6) or the increment and decrement keys.

Direct scanning allows frequencies within a predetermined frequency range (from F1 to F2) to be scanned. Utilizing the F1 key to enter the start frequency and F2 to enter the stop frequency, the scan range is set. The ΔF kHz key determines the size of the frequency step (1-1000 kHz). Time between frequency steps is set by depressing the SCAN DWL key and entering the dwell time via the numerical keys (01-99) or either the increment or decrement keys. The scan dwell range is selectable from 0.1 to 9.9 seconds in 0.1 second increments. After entering the start and stop frequencies, step size and the dwell time, depressing the SCAN STRT key begins the frequency scan. Scanning between the F1 and F2 frequencies continues until the SCAN STOP key is pressed. Depressing the SCAN STOP key halts the frequency scan at the frequency visible in the DEMOD display. Scanning is resumed by depressing the SCAN STRT key again.

Fine tuning (FINE TUNE) the unit allows for ± 50 Hz offset of the 3rd LO's 500 kHz frequency. Fine tuning provides the ability to compensate for frequency offsets. Depressing the FINE TUNE key enables the increment or decrement key to vary the fine tuning frequency, in 5 Hz steps. A minus sign (-) preceeds negative fine tuning frequencies. When FINE TUNE is offset, the front panel LED illuminates indicating that the tuned frequency is offset. Fine tuning offsets all six demodulators.

Bridging between the baseband inputs (A11J1-A11J6) allows more than one demodulator to process the same input baseband signal. Depressing the INP BRG key and then a pair of numbers (1-6), bridges the inputs from the first number entered through the second number entered. Bridging between demodulators 4 and 5 is accomplished via pressing the INP BRG key and then the 4 and 5 numerical keys. Bridging between all the demodulators is accomplished by enabling the bridging function and then pressing the 1 and 6 numeral keys. The 5 front panel LEDs illuminate, indicating the selection of bridging between all of the demodulators. Pressing the INP BRG key and then the 0 key removes any previously selected bridging between the demodulators.

2.4.2.3 CCITT Tuning

Tuning using the CCITT Plan is selected via the 960/2700 key. Pressing this multifunction key selects one of three tuning modes. The three tuning modes include: direct tuning, 960 Channel and 2700 Channel. Both the 960 and 2700 CCITT Plans cause the associated front panel LED to illuminate. With either CCITT Plan selected, the selected demodulator display will contain either 5 zeros (960 Channels) or 6 zeros (2700 Channels). Depressing the SMG, MG, SG, GP or CH key causes the decimal point to the right of one or two zeros on the DEMOD display to illuminate, indicating the number of digits to be entered. Refer to **Table 2-4** for the ranges of the two CCITT Plans.

Table 2-4. CCITT Tuning Plans**960 Channel Plan**

Selection	SG	GP	CH
Range	01-16	1-5	01-12
Display	14.	5.	08.

(Signifying Channel 8 of Group 5 in Supergroup 14 is selected.)

2700 Channel Plan

Selection	SMG	MG	SG	GP	CH
Range	1-3	7-9	4-8	1-5	01-12
Display	2.	9.	7.	3.	12.

(Signifying Channel 12 of Group 3 of Supergroup 7 of Mastergroup 9 from Supermastergroup 2 is selected.)

Since both the 960 and 2700 Channel Plans function essentially the same way, only the 2700 Channel Plan operation is discussed.

Pressing the 960/2700 key until the front panel LED for the 2700 Channel Plan illuminates, selects the 2700 CCITT Plan. The selected DEMOD display indicates all zeros. Pressing the SMG key enables the numerical keys to select a SMG (1-3). The selected SMG number is entered to the left of the pulsing decimal point. Likewise with the selection of the MG, SG, GP and CH keys, the decimal point to the right of the digit(s) to be entered flashes until the required number of digits is entered.

NOTE

Entering a numerical value that is beyond the established CCITT range for each parameter causes an audible tone to be generated when the erroneous CCITT frequency is attempted to be entered via depressing the TUNE key.

Pressing the TUNE key causes the valid CCITT Plan frequency to be entered and tunes the demodulator to the selected frequency. Holding the TUNE key depressed displays the direct tuned frequency. Releasing the TUNE key again displays the tuned CCITT Plan for frequency in the selected DEMOD display.

NOTE

Cycling the tuning mode through direct tuning and back to either CCITT Plan causes both the 2700 and 960 Channel Plans to display all zeros.

With the demodulator tuned to a valid CCITT Plan frequency, the tuned frequency can be varied via depressing the group or channel key for the parameter (channel, group, etc.) to be changed and then pressing either the increment or decrement key. After the group or channel key has been pressed, the increment or decrement key is utilized to vary the selected group or channel. When the channel or group is stepped beyond its limit, an audible tone is heard and the DEMOD displays the last valid frequency entered.

Scanning for the selected CCITT Plan is provided via depressing the SCAN STRT key. Scanning starts at the selected channel and continues up to channel 12. When channel 12 has been swept, the scanning starts again at channel 1. If the channels of another group are desired to be scanned, the group key (SMG, MG, SG or GP) is depressed and then either the increment or decrement key is depressed to select another group for scanning. Scanning for the CCITT Plan is only by channel, in 4 kHz steps.

2.4.3 REMOTE OPERATION

2.4.3.1 Remote Control

Remote control allows the selected demodulator parameters to be updated or verified via a remote controller connected to the IEEE-488 connector (J1). Address switch S1 of the IEEE-488 Interface subassembly (A9A2) determines the unit address. **Table 2-5** indicates the switch setting for the associated address. The WJ-9518BE-9S address switch setting is read by the microprocessor when the unit is powered up. Changing the unit address requires the address switch (S1) to be changed and the unit power to be turned off and then turned on again; simply changing the address switch does not change unit address that is stored in memory. Without turning the unit power off and back on again, the unit only responds to the address that was set at the time the unit was energized.

With the IEEE-4888 subassembly (A9A2) option switch (S2) most significant bit switch position closed (ON), the unit's 488 address can be changed without having to reset the switch settings of the address switch (S1). With the most significant bit of S2 closed (ON), the front panel keyboard can be used to change the 488 address of the unit. To determine the unit's 488 address, press the DEM SEL key and the 0 key. The three demodulator displays (DEMOD 1 through and DEMOD 3) display "IEEE" (in DEMOD 1) "-488" (in DEMOD 2) and "XX" (in DEMOD 3). The "XX" indicates any number from 0 to 30. After the 488 address indications are displayed with the demodulator displays, the increment and decrement keys are used to control the displayed 488 address. With the desired 488 address displayed, turn the unit power off and back on again to enter the new address into memory.

If, during the time the 488 address is being set by the front panel, the address set by switch S1 is the desired address pressing the DEM SEL key and the 1 key exits the address selection mode.

Utilizing the remote commands listed in **Table 2-6**, all of the demodulator parameters are controllable via the remote controller. The commands are listed in order of priority. Write and Read statements utilized to change and request demodulator parameters do not recognize or use spaces or decimal points.

2.4.3.2 Write Statement

When a device on the IEEE-488 BUS is written to, the following format should be followed. A control statement requires: the statement **OUTPUT** (Write), the controller address (X), the device address (XX), quotation marks ("), the demodulator affected, the parameter(s) to be set and the closing quotation marks ("). A Write statement is utilized to change the selected demodulator status one parameter at a time or a group (string) of parameters at one time. When a string of parameters is to be changed, use semicolons (;) between the parameters being changed. The WJ-9518BE-9S buffer accepts only 65 characters at a time before generating an error code (01). A typical Write statement to select a demodulator and set a string of parameters would be as follows:

OUTPUT 706; "DEM1; FRQ 10000; UPR; RFG0; BRG 1 6"

This Write statement contains: the type of statement WRT (write), the controller address (7), the device address (06), a semicolon (;), quotation marks (" ") around the demodulator selected and parameters to be changed. Parameters changed are selecting DEMOD 1, setting the TUNED FREQ to 10000 kHz, Upright detection mode, RF GAIN to minimum and BRIDGING between demodulators 1-6. An error in the Write statement causes any parameter changes, from the error until the end of the statement, to not be accepted by the unit. Another Write statement, with valid parameters, must be sent to update the parameters that were not changed because of the invalid command statement. **Table 2-5** lists the format utilized for Write statements.

NOTES

When a command string contains an error and is sent to the FDM Demodulator, any parameter change(s) from the error on is (are) not processed by the unit.

The "CLR" command should be sent alone and not in a command string.

Table 2-5. S1 Address Selection

Address	Switch Position							
	1	2	3	4	5	6	7	8
0	O	O	O	O	O	O	O	O
1	X	O	O	O	O	O	O	O
2	O	X	O	O	O	O	O	O
3	X	X	O	O	O	O	O	O
4	O	O	X	O	O	O	O	O
5	X	O	X	O	O	O	O	O
6	O	X	X	O	O	O	O	O
7	X	X	X	O	O	O	O	O

O = Open = Off = 0
X = Closed = On = 1

Table 2-5. S1 Address Selection (Cont'd)

Address	Switch Position							
	1	2	3	4	5	6	7	8
8	O	O	O	X	O	O	O	O
9	X	O	O	X	O	O	O	O
10	O	X	O	X	O	O	O	O
11	X	X	O	X	O	O	O	O
12	O	O	X	X	O	O	O	O
13	X	O	X	X	O	O	O	O
14	O	X	X	X	O	O	O	O
15	X	X	X	X	O	O	O	O
16	O	O	O	O	X	O	O	O
17	X	O	O	O	X	O	O	O
18	O	X	O	O	X	O	O	O
19	X	X	O	O	X	O	O	O
20	O	O	X	O	X	O	O	O
21	X	O	X	O	X	O	O	O
22	O	X	X	O	X	O	O	O
23	X	X	X	O	X	O	O	O
24	O	O	O	X	X	O	O	O
25	X	O	O	X	X	O	O	O
26	O	X	O	X	X	O	O	O
27	X	X	O	X	X	O	O	O
28	O	O	X	X	X	O	O	O
29	X	O	X	X	X	O	O	O
30	O	X	X	X	X	O	O	O

O = Open = Off = 0

X = Closed = On = 1

2.4.3.3 Read Statement

Read statements follow the format similar to the Write statement. The only difference is the use of **ENTER** (for read) and the use of a question mark to indicate the request of a parameter status. As with the Write statement, only the status of the selected demodulator is output in response to the Read statement. When WJ-9518BE-9S receives a Read statement, it takes control of the IEEE-488 BUS, becoming a "talker" and outputs the requested data onto the BUS. After the data output is completed, the unit relinquishes control of the BUS and once again becomes a "listener". To read a parameter status, the following procedure should be followed after dimensioning the array: Example DIM R\$ [30].

Request the desired parameter	ENTER 706; "FRQ?"
Read the data string	ENTER 706; R \$
Display the data string	DSP R \$
or	
Print the data string	PRT R \$

Table 2-6 lists the format utilized for Read statements. Only the last parameter queried in a Write statement is displayed on the HP-85. Each parameter must be verified separately. Responses to parameter queries are for the demodulator last addressed via the

OUTPUT command. Thus a query may be preceded by a command statement to select the desired demodulator.

Table 2-6. Remote Control Commands and Responses

Command	Response	Description	Range
DEM (a)		DEMOD Selected	a = 1-6
DEM?	DEM_(a)	Query Selected DEMOD	a = 1-6
FRQ (aaaaaa)		FREQUENCY set	a = 0-15000 (in kHz)
FRQ?	FRQ_(aaaaaa)	Query FREQUENCY	a = 0-15000 (in kHz)
UPR		Upper Sideband Select	
INV		Inverted Sideband Select	
SB?	UPR or INV	Query Sideband Selected	
RFG (aaa)		RF GAIN Set	a = 001-127
RFG?	RFG_(aaa)	Query RF GAIN	a = 001-127
FT (±aa)		FINE TUNE Set	a = ±0-50 (in 5 Hz steps)
FT?	FT_(±aa)	Query FINE TUNE	a = ±0-50 (in 5 Hz steps)
BRG (a-a a-a, a-a a-a, a-a, a-a)		INPUT BRIDGING Select	a = 0-6
RMT		REMOTE Control Select	
RMT/		LOCAL Control Select	
RMT?	RMT or RMT/	Query Control Status	
CLR		Master Reset; Sets all parameters to initialized values (page 2-4)	
ERR?	ERR_(aa)	Query Error Number	a = 00-99
VER?	VER_(14 a's)	Query Software Version	a = 9518BE9S 1.0.0
FRA (aaaaaa)		F1 (Start Frequency) Set	a = 0-15000 (in kHz)
FRA?	FRA_(aaaaaa)	Query F1 (Start Frequency)	a = 0-15000 (in kHz)
FRB (aaaaaa)		F2 (Stop Frequency) Set	a = 0-15000 (in kHz)
FRB?	FRB_(aaaaaa)	Query F2 Stop Frequency	a = 0-15000 (in kHz)
SIZ (aaaa)		Frequency Step Size Set	a = 0-1000 (in kHz)
SIZ?	SIZ_(aaaa)	Query Frequency Step Size	a = 0-1000 (in kHz)
DWL (a.a)		DWELL Time Set	a = 0.2-9.9 (in sec.)
DWL?	DWL_(a.a)	Query DWELL Time	a = 0.2-9.9 (in sec.)
SCN		SCAN START	
SCN/		SCAN STOP	
SCN?	SCN or SCN/	Query SCAN Status	
CTA (aa,a,aa)		Selected CCITT 960 Channel Plan	aa = 01-16, a = 1-5, aa = 01-12
CTB (a,a,a,a,aa)		Selected CCITT 2700 Channel Plan	a = 1-3, a = 7-9, a = 4-8, a = 1-5, aa = 01-12
CT?	CTA (aa,a,a,aa) or CTB (a,a,a,aa)	Query CCITT Plan	
CT/		Returns to direct frequency mode	

Table 2-6. Remote Control Commands and Responses (Cont'd)

Command	Response	Description	Range
SMG (a)		Supermastergroup Select	a = 1-3 (2700 CH Plan Only)
SMG?	SMG_(a)	Query Supermastergroup Select	a = 1-3 (2700 CH Plan Only)
MG (a)		Mastergroup Select	a = 7-9 (2700 CH Plan Only)
MG?	MG_(a)	Query Mastergroup	a = 7-9 (2700 CH Plan Only)
SG (aa) or (a)		Supergroup Select	aa = 01-16 (960 CH Plan) a = 4-8 (2700 CH Plan)
SG?	SG_(aa) or (a)	Query Supergroup	aa = 0-16 (960 CH Plan) a = 4-8 (2700 CH Plan)
GP (a)		Group Select	a = 1-5
GP?	GP_(a)	Group Query	a = 1-5
CH (aa)		Channel Select	aa = 01-12
CH?	CH_(aa)	Channel Query	aa = 01-12
FPL		Enables Front Panel Display	
FPL/		Front Panel Disable (Blanks all LEDs except RMT)	
FPL?	FPL or FPL/	Query Front Panel Status	
STS?	STS_(aaa)	Status Request	aaa = 001-008 (see Table 2-7)

(a) Represents an ASCII number

Table 2-7 indicates the significance of each of the four bits used of a serial poll status byte. When a bit is set, is HIGH, the corresponding indication in **Table 2-7** is true. Clearing a bit that has been set is accomplished via the commands listed in **Table 2-7**.

Table 2-7. Status Byte Serial Poll

Bit Displayed	Set Indicates	Clear Indicates	Cleared By
0	Not Used	-	-
1	Power Up SRQ	-	STS?
2	Not Used	-	-
3	Not Used	-	-
4	Processing Message or Response to a Request for Data is Available in the Buffer	No 488 Action Pending	Cleared after message is processed or After Talking
5	Error Condition	No Error Condition	ERR?
6	SRQ	No SRQ	Serial Poll
7	Not Used	-	-

Utilizing the ASCII format listed in **Table 2-6**, the following tables indicate the data transfer sequence taking place on the IEEE-488 BUS. **Table 2-8** illustrates the bus sequence when a command is sent to the WJ-9518BE-9S.

Table 2-8. Sending a Tuned Frequency Response

Message: Tune DEMOD 1 to 15 MHz

ASCII Mode	Actual Bus Transfer					
	Byte	ATN	EOI	HEX	ASCII	Comment
Output 706 using "K"; "DEM1; FRQ15000" AN ASCII message may have leading zeroes	1	1	0	3F		UNLISTED
	2	1	0	55		HP-85 TALK
	3	1	0	26		9518 LISTEN
	4	0	0	44	D	DATA SENT
	5	0	0	45	E	DATA SENT
	6	0	0	4D	M	DATA SENT
	7	0	0	31	1	DATA SENT
	8	0	0	3B	;	DATA SENT
	9	0	0	46	F	DATA SENT
	10	0	0	52	R	DATA SENT
	11	0	0	51	Q	DATA SENT
	12	0	0	31	1	DATA SENT
	13	0	0	35	5	DATA SENT
	14	0	0	30	0	DATA SENT
	15	0	0	30	0	DATA SENT
	16	0	0	30	0	DATA SENT
	17	0	0	0D	CR	DATA SENT
	18	0	0	0A	LF	TERMINATOR

NOTES

F = The controller address

06 = The WJ-9518BE-9S address

K = limits the string by eliminating blank characters

Table 2-9 illustrates the status of the interface bus as the WJ-9518BE-9S responds to a query from the controller. In order to verify that DEMOD 1 responded properly to the remote command, the unit is queried.

Table 2-9. Response to a Frequency Query

Message: Send the tuned frequency of DEMOD 1

ASCII Mode	Actual Bus Transfer					
	Byte	ATN	EOI	HEX	ASCII	Comment
Output 706 using "K", "DEM1; FRQ?" Prepares the unit to respond to the query when made a talker	1	1	0	3F		UNLISTEN
	2	1	0	55		HP85 TALK
	3	1	0	26		9518 LISTEN
	4	0	0	44	D	DATA to 9518
	5	0	0	45	E	DATA to 9518
	6	0	0	4D	M	DATA to 9518
	7	0	0	31	1	DATA to 9518
	8	0	0	3B	;	DATA to 9518
	9	0	0	46	F	DATA to 9518
	10	1	0	52	R	DATA to 9518
	11	1	0	51	Q	DATA to 9518
	12	1	0	3F	?	DATA to 9518
	13	0	0	0D	CR	DATA to 9518
	14	0	0	0A	LF	TERMINATOR
	15	0	0	3F		UNLISTEN
	16	0	0	35		HP85 LISTEN
	17	0	0	46		9518 TALK
	18	0	0	44	D	DATA from 9518
	19	0	0	45	E	DATA from 9518
	20	0	0	4D	M	DATA from 9518
	21	0	0	31	1	DATA from 9518
	22	0	0	3B	;	DATA from 9518
	23	0	0	46	F	DATA from 9518
	24	0	0	52	R	DATA from 9518
	25	0	0	51	Q	DATA from 9518
	26	0	0	31	1	DATA from 9518
	27	0	0	35	5	DATA from 9518
	28	0	0	30	0	DATA from 9518
	29	0	0	30	0	DATA from 9518
	30	0	0	30	0	DATA from 9518
	31	0	0	0D	CR	DATA from 9518
	32	0	0	0A	LF	TERMINATOR

2.4.3.4 Remote Error Codes

The following list briefly describes the cause for the displayed error code. Displayed error codes do not display the most significant digit (4).

<u>Remote Error Code</u>	<u>Description</u>
Err 401	Buffer is full.
Err 404	Number is out of range for command.
Err 407	Invalid mnemonic or binary code received.
Err 440	Command not valid during present mode of operation.

2.4.3.5 Fatal Error Codes

During unit operation two errors can occur that cause the unit operation to cease. These errors prohibit further unit operation until the cause of the error is eliminated. The errors are displayed via the DEMOD 1 LEDs as:

- Error 1 - for a fatal software error
- Error 2 - for a RAM read or write error

Turning the unit power off and then powering the unit up again may clear the error if the error was only temporary. If the fatal error still exists, turn the unit power off and press the REMOTE key while the unit power is turned on again.

2.5 PREPARATION FOR RESHIPMENT

In the event that reshipment is necessary, follow the packaging methods utilized for the original shipment. If the original packaging container and materials have been retained, and are in good condition, they may be reused. If not reused, the original packaging may provide, at minimum, guidance for the repackaging effort.

FIGURE 2-3

WJ-9518BE-9S

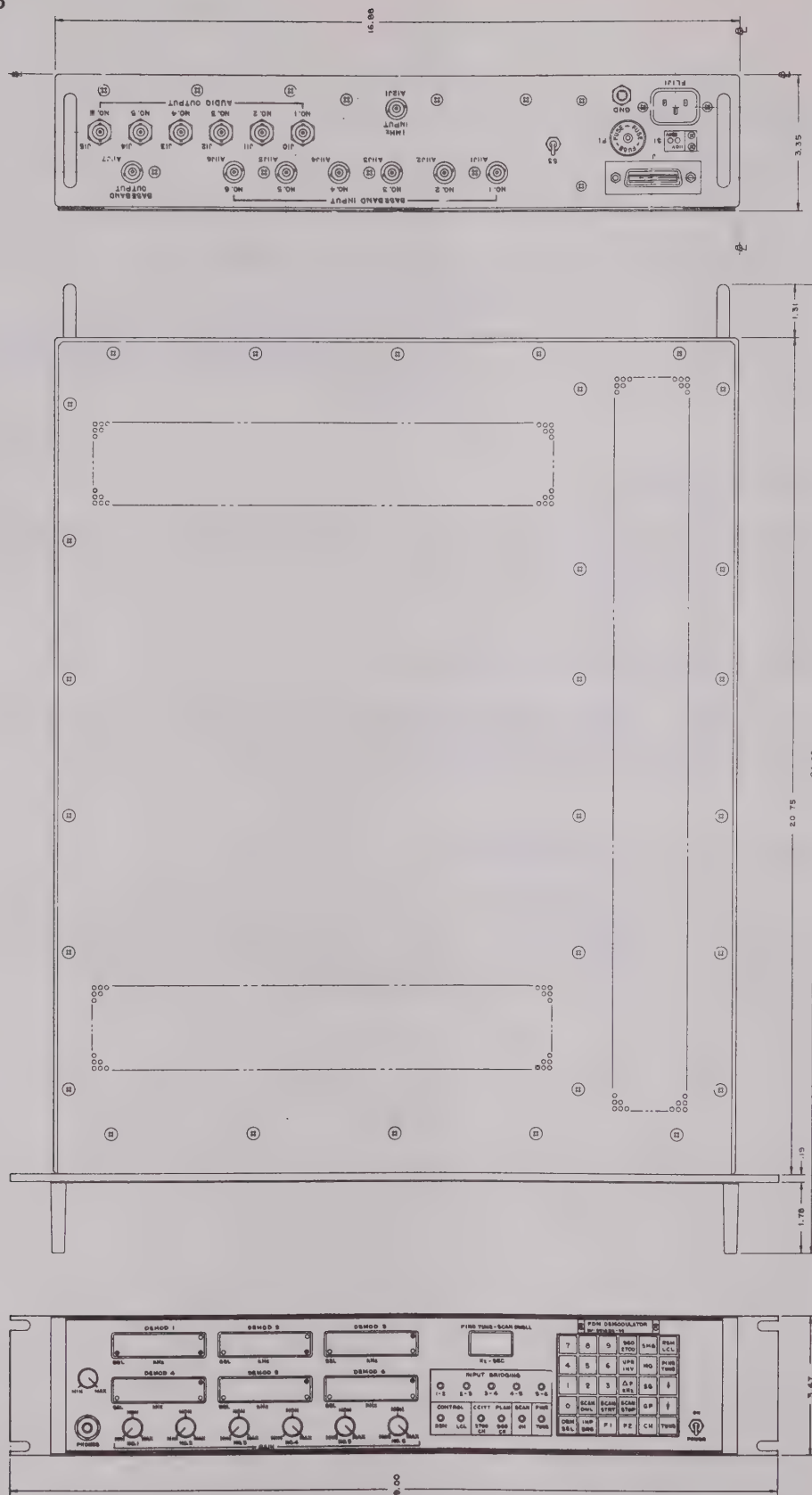
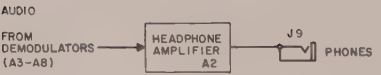
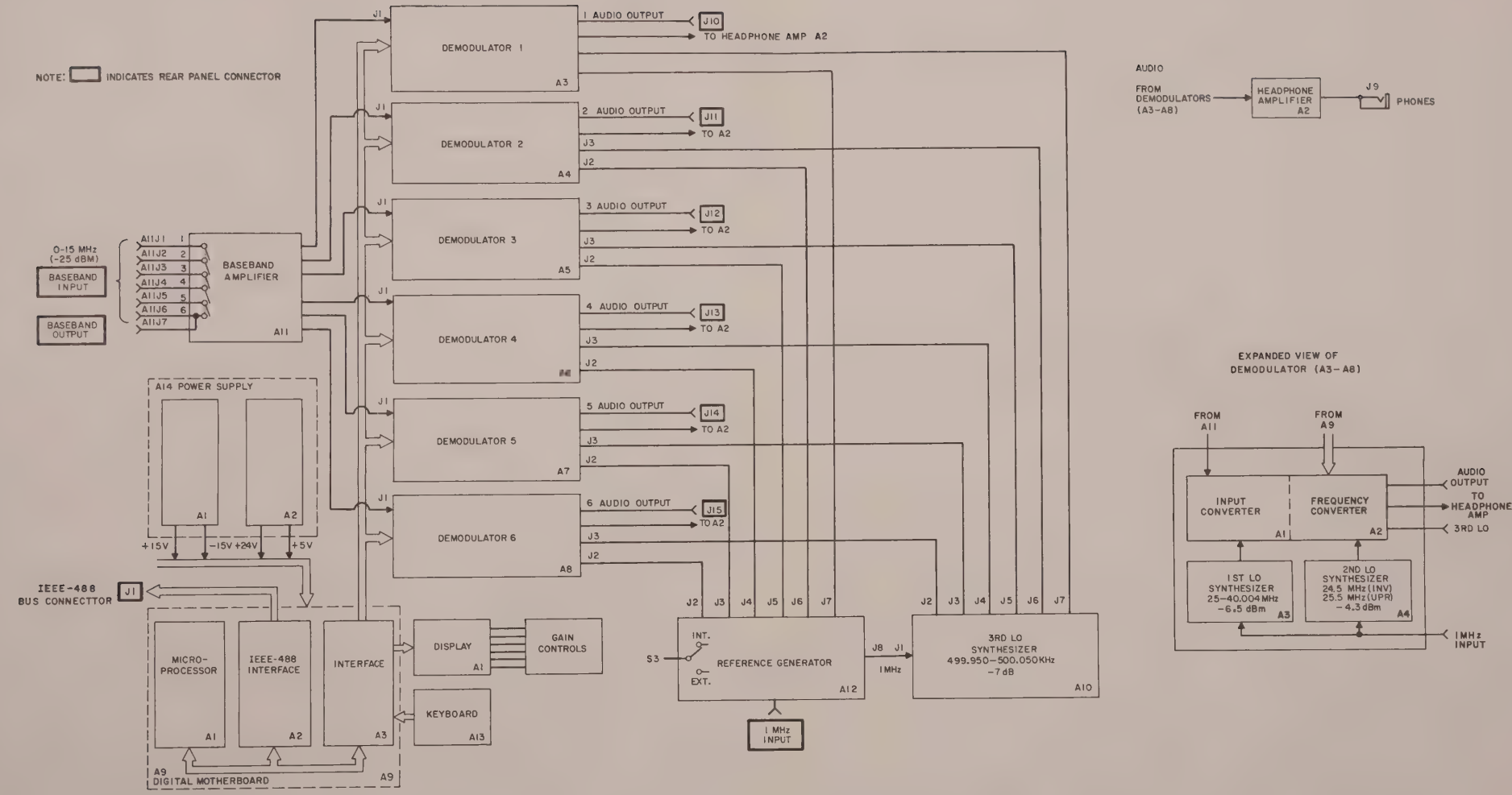


Figure 2-3. WJ-9518BE-9S Outline Drawing

SECTION III
CIRCUIT DESCRIPTION

FIGURE 3-1



EXPANDED VIEW OF DEMODULATOR (A3-A8)

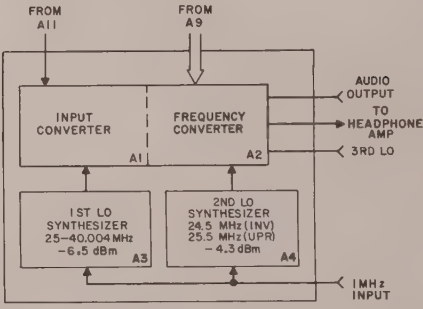


Figure 3-1. WJ-9518BE-9S FDM Demodulator Block Diagram

SECTION III

CIRCUIT DESCRIPTION

3.1 GENERAL DESCRIPTION

The WJ-9518BE-9S FDM Demodulator receives and demodulates baseband signals from 0-15 MHz that are applied to the BASEBAND INPUT connectors (A11J1-A11J6). Input baseband signals can be demodulated independently or bridged together allowing from one to six of the more than one Demodulator assemblies (A3-A8) to demodulate the same signal. Baseband Amplifier A11 provides either an independent or bridged signal path for the input baseband signal to the Demodulator assemblies (A3-A8). Connector A11J7 provides a output sample of the baseband signal applied to A11J6. Baseband signals applied to the Demodulator assemblies (A3-A8) are filtered by the Input Converter's low-pass filter. Refer to **Figure 3-1** for the WJ-9518BE-9S block diagram. Filtered baseband signals from the Input Converter are mixed with the 1st LO Synthesizer output frequency (25-40.004 MHz) to produce the 25 MHz 1st IF. Mixing the 1st IF frequency with the 24.5 MHz (INV) or 25.5 MHz (UPR) 2nd LO frequency, from the 2nd LO Synthesizer (AXA4), produces the 2nd IF of 500 kHz. Mixing the 3rd LO frequency (499.950-500.050 kHz) with the 500 kHz 2nd LO produces the 0-3850 Hz at the AUDIO OUTPUT connectors (J10-J15).

The Reference Generator Assembly (A12) provides a 1 MHz reference for the LO synthesizer circuits. Rear panel switch S3 enables selection of either an internal ovenized crystal oscillator reference (U1) or an external 1 MHz reference source. Depending on the switch setting of S3, either the internal (INT) or external (EXT) reference is selected.

Control of the WJ-9518BE-9S FDM Demodulator is accomplished via the three digital subassemblies that plug into the Digital Motherboard (A9). The Digital Motherboard provides for either local or remote control. Local control is provided via the Keyboard assembly (A13) with the parameter status being displayed on the front panel Display assembly (A1). Remote control is provided via connecting a remote controller device to the IEEE-488 bus connector (J1).

Reference should be made to the functional block diagrams provided in this section and also to the schematic diagrams, provided in **Section VI**, as a supplement to the following circuit descriptions.

The unit numbering method utilized throughout this unit for identification of electrical components within this demodulator is as follows. Components on the various subassemblies carry a prefix in addition to the usual class letter and component designation; such as A3A1 or A4A1Q1. These subassembly prefixes are omitted in the circuit description and illustrations, except when confusion could result because of their omission.

3.2 FUNCTIONAL DESCRIPTION

Reference Generator A12 produces a 1 MHz signal that is applied to the 3rd LO Synthesizer (A10) and also to the 1st LO and 2nd LO Synthesizers of each Demodulator assembly A3-A8. **Figure 3-2** illustrates the Reference Generator block diagram. The 1 MHz reference signal from A12 can be derived internally or from an external 1 MHz signal applied to connector J1. Rear panel reference selection switch S3 determines whether the reference

utilized is from an external source or from the internal oscillator (U1). Selecting the external reference applies the 1 MHz signal through transistor Q1 and Q2, through multiplexer U2 and through inverters U3 and U4 to the Demodulator assemblies (A3-A8) via J2 through J7 and also to the 3rd LO Synthesizer (A10) via J8. Selecting the internal reference applies the 10 MHz crystal oscillator output through frequency divider U1 and then through U2, U3 and U4 to the outputs (J2-J8).

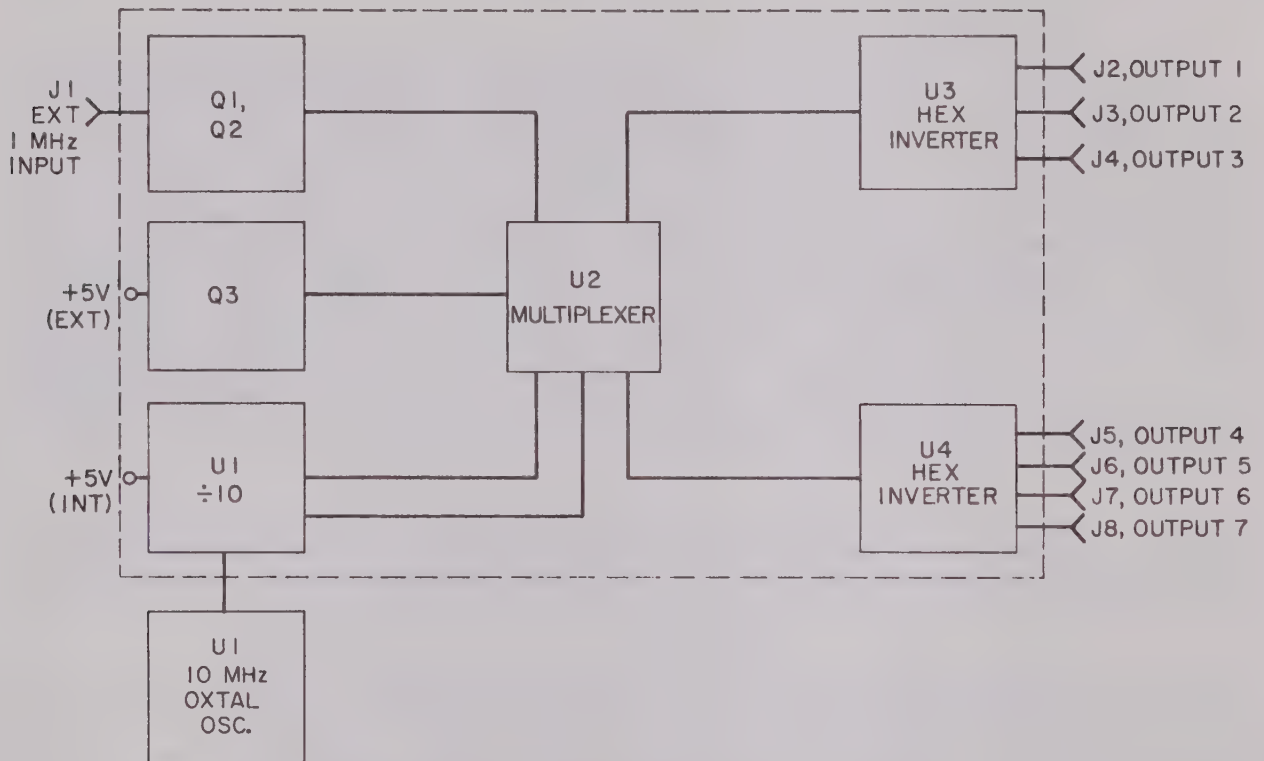


Figure 3-2. Reference Generator Block Diagram

Baseband Amplifier A11 receives baseband signals between 0 and 15 MHz with a nominal input level of -25 dBm. Received baseband signals are applied to BASEBAND INPUTS A11J1-A11J6. The block diagram for the Baseband Amplifier is illustrated in **Figure 3-3**. Baseband signals at Input 1 are applied to the Baseband Amplifier buffer 1 circuit. Signals at the other five baseband inputs are applied respectively to relays K1 through K5 before being applied to buffers 2 through 6. These five relays are energized via data applied through U3, U1 and the Baseband Amplifiers output drivers. Energizing the relay allows the baseband signal at one input to be applied to more than one demodulator via selecting bridging. Bridging allows two to six Demodulator assemblies to process the same input baseband signal. BASEBAND OUTPUT A11J7 provides a buffered output of the baseband signal applied to A11J6.

Each baseband output from the Baseband Amplifier, J8-J13, is applied to the associated Demodulator assembly (A3-A8). Input baseband signals are applied to J1 of the selected Demodulator assembly. Refer to **Figure 3-4** for the Demodulator block diagram. Each of the six Demodulator assemblies are identical. Demodulators contain four subassemblies: Input Converter AXA1, Frequency Converter AXA2, 1st LO Synthesizer AXA3 and 2nd LO Synthesizer AXA4.

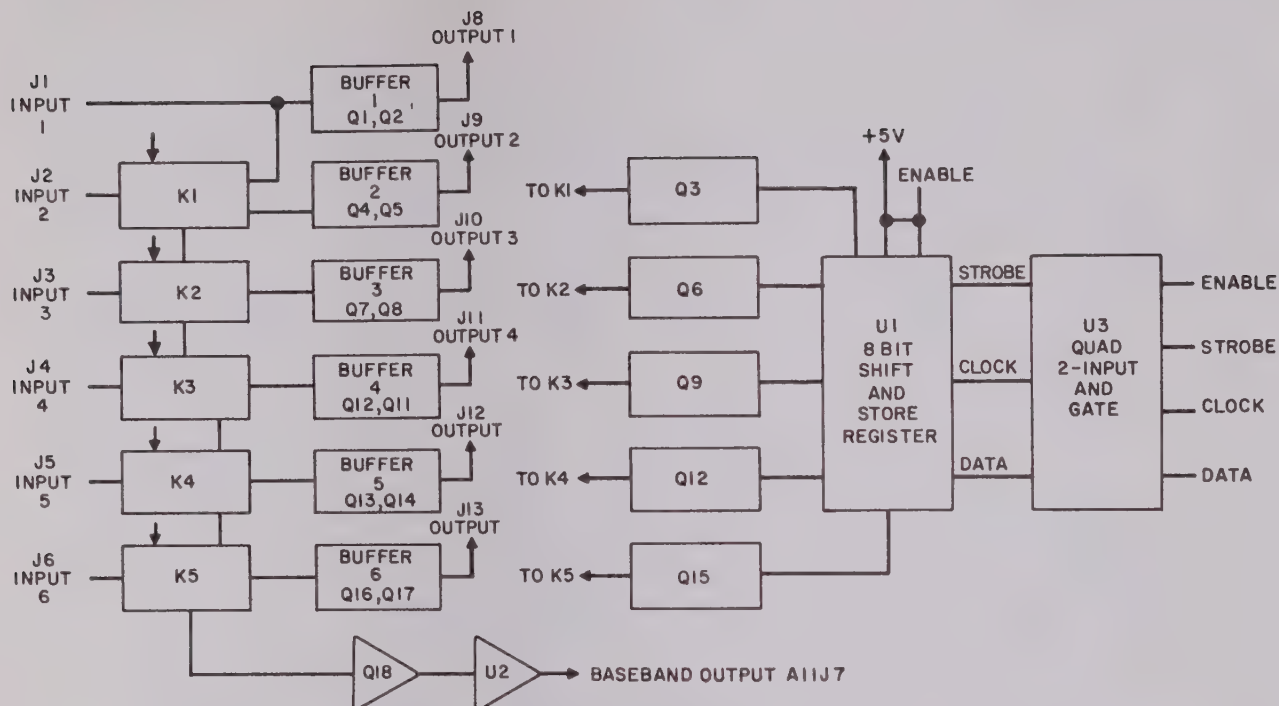


Figure 3-3. Baseband Amplifier Block Diagram

Baseband signals are applied to J1 of the Input Converter subassembly (AXA1). (Refer to **Figures 3-4** and **3-5** for the Input/Frequency Converter block diagram.) Baseband signals are filtered through a low-pass filter (L1-L3 and C1-C10) before being applied as one input of mixer U2. The other input to mixer U2 is the 1st LO frequency. Mixer products from the Input Converter are applied to the Frequency Converter subassembly (AXA2). Input signals applied to the Frequency Converter from the Input Converter are filtered through filter FL1 to produce the 1st IF of 25 MHz. The 1st IF is amplified before being applied as one input of mixer U4. The 2nd LO, amplified via U5, is the other input to mixer U4 to produce the 500 kHz 2nd IF. Mixer products are amplified and filtered via FL2 that passes the upper sideband frequencies of 500-504 kHz. Transistors Q3 and Q4 provide further amplification of the 2nd IF before being applied to mixer U9. U9 mixes the 2nd IF with the 3rd LO frequency to produce the difference frequencies of 300-3850 Hz. Output mixer signals are amplified and equalized before being applied to the audio output.

Data applied to U8 from the Digital Motherboard (A9) is utilized when the gain level is changed. Data applied to U8 is coupled through U7 to digital-to-analog converter U6. U6 produces an output voltage proportional to the binary equivalent applied at the input of digital-to-analog converter U6. The output voltage from U6 controls the gain of transistor amplifier Q1.

1st LO frequencies applied to the Input Converter are synthesized via the 1st LO Synthesizer (AXA3). Refer to **Figure 3-6** for the 1st LO Synthesizer block diagram.

The 1st LO Synthesizer subassembly utilizes phase lock loop circuitry to synthesize the 1st LO tuned frequencies. The phase lock loop utilizes the 1 MHz reference signal from the Reference Generator (A12) as the reference frequency for the phase lock loop (PLL). A voltage controlled oscillator tunes the 1st LO frequency from 25 MHz to 40.004 MHz in 1 kHz steps.

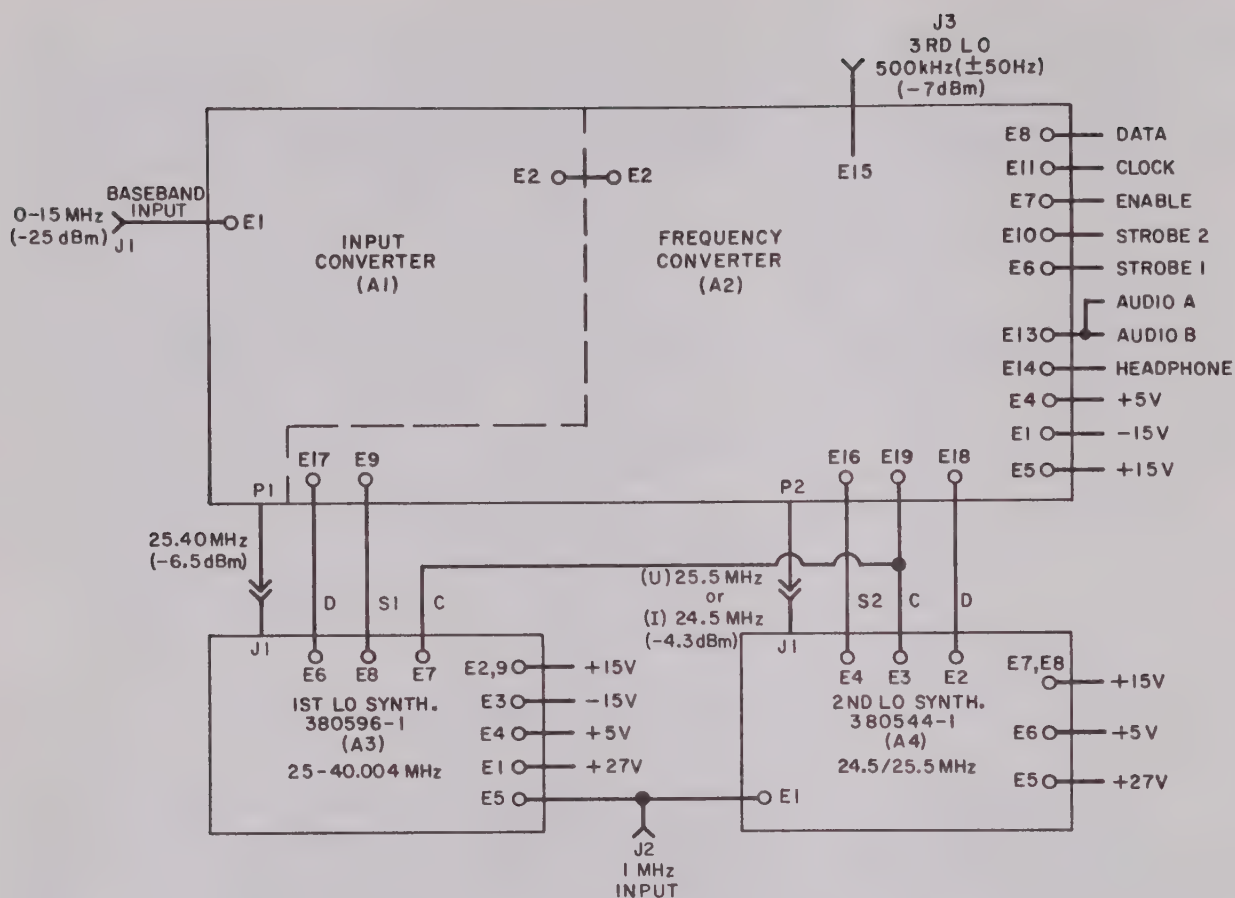


Figure 3-4. Demodulator Block Diagram

Frequency synthesis is accomplished via phase lock loop frequency synthesizer U2. U2 compares the 1 MHz reference frequency and digitally encoded frequency data input to shift and store register U3 and to frequency synthesizer U2. Input data applied through U3 to U2 is stored in U2's internal registers. U2 divides the reference and digital frequencies and then compares the frequency and phase of the two resultant frequencies. Any difference causes U2 to apply an error signal to operational amplifier U4. Output voltages from U4 drive variable capacitance diodes that tune the frequency of transmission line oscillator Q1. Oscillator frequencies applied through U5 are divided by either 80 or 81, dependent upon the output level of the control line from U2. Oscillator frequencies are also applied to frequency dividers U8 and U9. Selection of frequency divider U8 or U9 is determined by output levels from U3 enabling the transistors, Q2 for U8 and Q3 and Q4 for U9, to allow either U8 or U9 to be selected. Output frequencies from these frequency dividers are coupled from U5 to frequency synthesizer U2 and from U8 or U9 to J2 after being filtered and amplified.

The 2nd LO Synthesizer provides a fixed output frequency of either 24.5 MHz or 25.5 MHz. Refer to **Figure 3-7** for the 2nd LO Synthesizer block diagram.

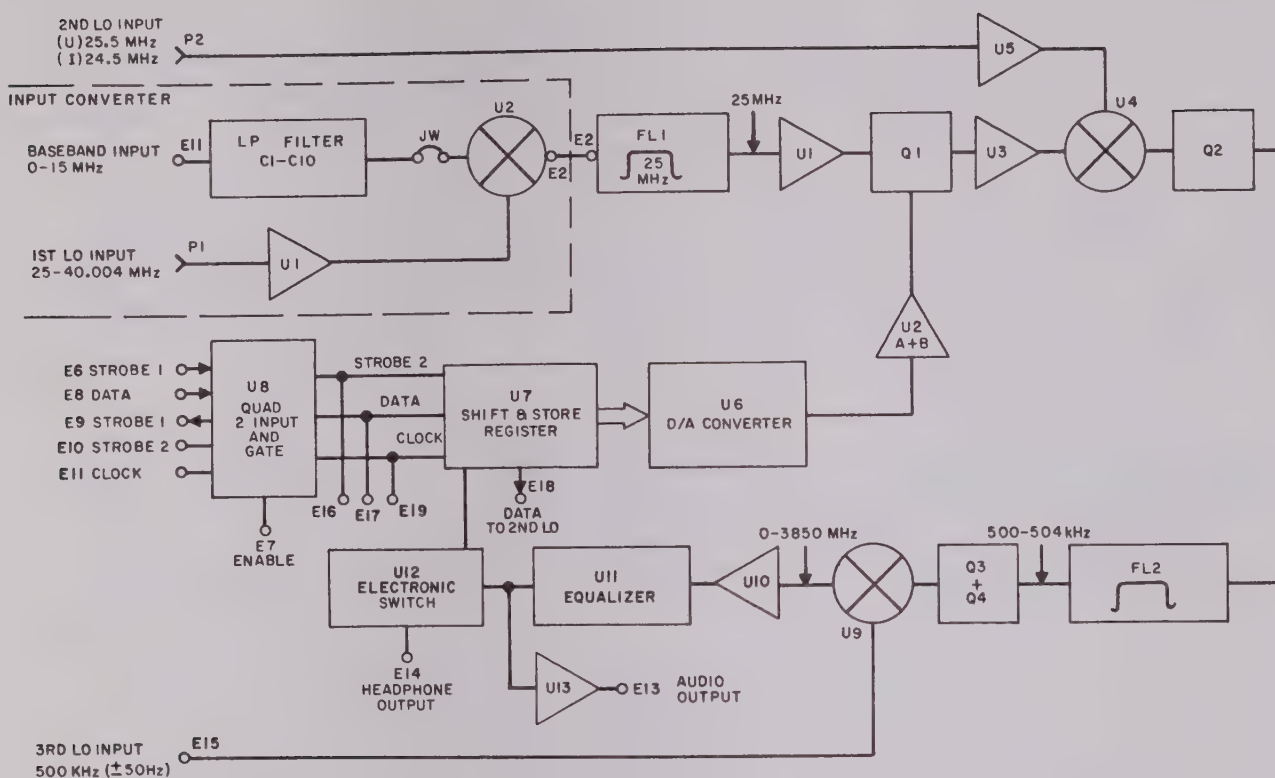


Figure 3-5. Input/Frequency Converter Block Diagram

2nd LO Synthesizer subassembly A3A4-A8A4 produces the 2nd LO frequency of 24.5 MHz (Inverted mode) or 25.5 MHz (Upright mode). Frequency synthesis of the 2nd LO is accomplished via phase lock loop frequency synthesizer U2. Frequency data, at E2, applied to U2 is divided and compared with the divided 1 MHz reference frequency. Differences in either frequency and/or phase causes U2 to generate an error signal that is amplified through U3 and applied to varicap diodes in the transmission line circuitry. The varicap diodes are utilized to tune the frequency of the transmission line oscillator. Oscillator frequencies are split and applied to frequency dividers U4 and U5. U4 divides the oscillator frequency by 80 or 81 and U5 divides input frequencies by 10. Output frequencies from U4 are applied to U2 to complete the phase lock loop. Frequencies output from U5 are filtered, amplified, and filtered again before being applied out J1 to the Frequency Converter subassembly (A2).

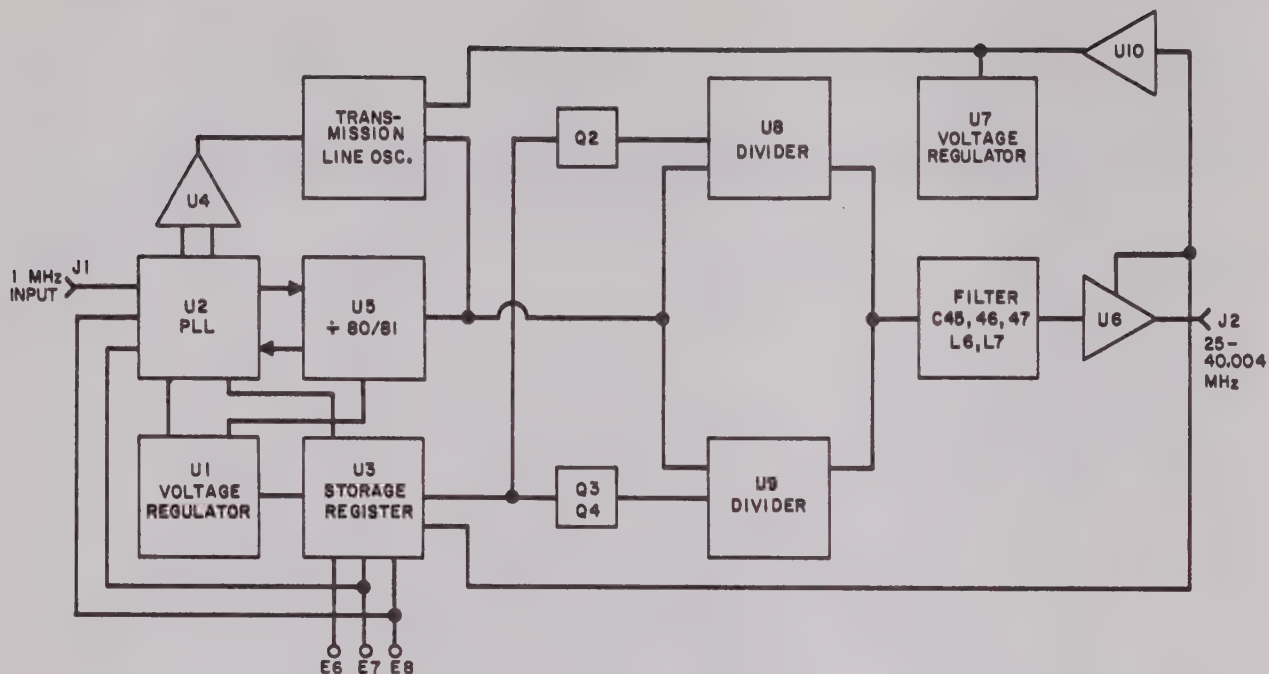


Figure 3-6. 1st LO Synthesizer Block Diagram

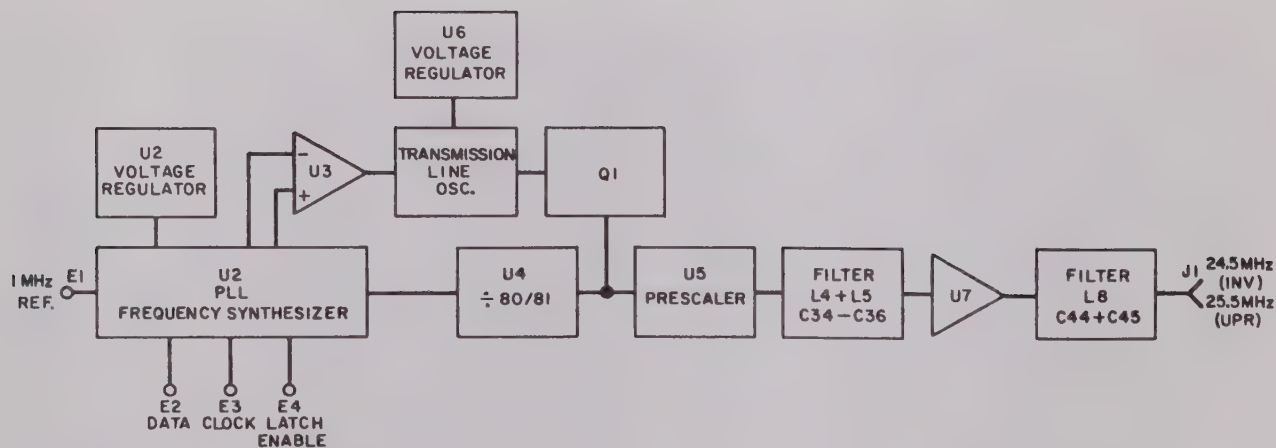


Figure 3-7. 2nd LO Synthesizer Block Diagram

The 3rd LO Synthesizer assembly provides the 500 kHz ± 50 Hz 3rd LO frequency to the Frequency Converter subassembly. **Figure 3-8** illustrates the 3rd LO Synthesizer as a block diagram.

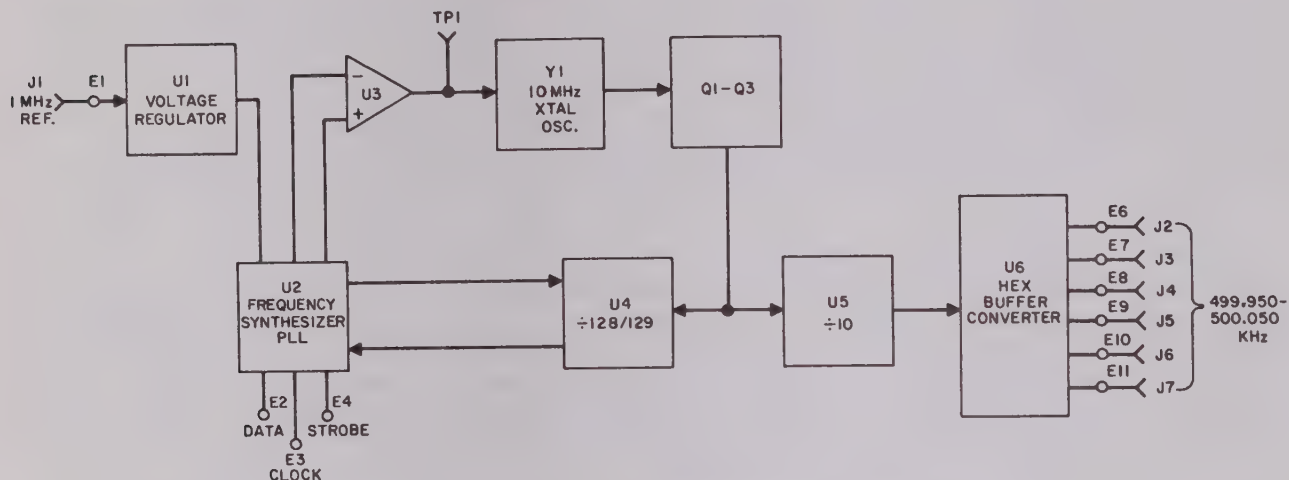


Figure 3-8. 3rd LO Synthesizer Block Diagram

The 3rd LO frequencies are synthesized from data applied to phase lock loop frequency synthesizer U2. U2 divides and compares the 1 MHz reference frequency with the divided by 128 or 129 (via U4), 10 MHz oscillator frequency. Detected differences in frequency and/or phase cause an error signal from U2 to be amplified through U3. Error voltages from U3 are utilized to tune the frequency of the oscillator by varying the capacitance of the varicap diodes. Transistors Q2 and Q3 amplify the oscillator signal before it is split and applied to two frequency dividers U4 and U5. U4 divides the oscillator frequency by either 128 or 129 before being applied to U2. U5 divides the oscillator frequency by 10 and applies the divided oscillator frequency, inverted through hex buffer U6 and applied to the Frequency Converter subassembly.

Headphone Amplifier assembly A2 amplifies the output demodulator audio signal of the selected demodulator. **Figure 3-9** illustrates the Headphone Amplifier in block diagram form.

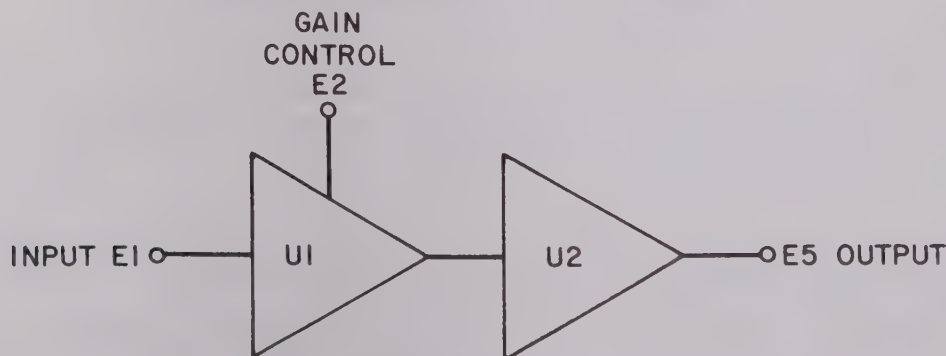


Figure 3-9. Headphone Amplifier Block Diagram

The Keyboard (A13) contains a 30 pushbutton keypad and is utilized to select and control the unit operating parameters during local control. **Figure 3-10** illustrates the Keyboard switch circuitry.

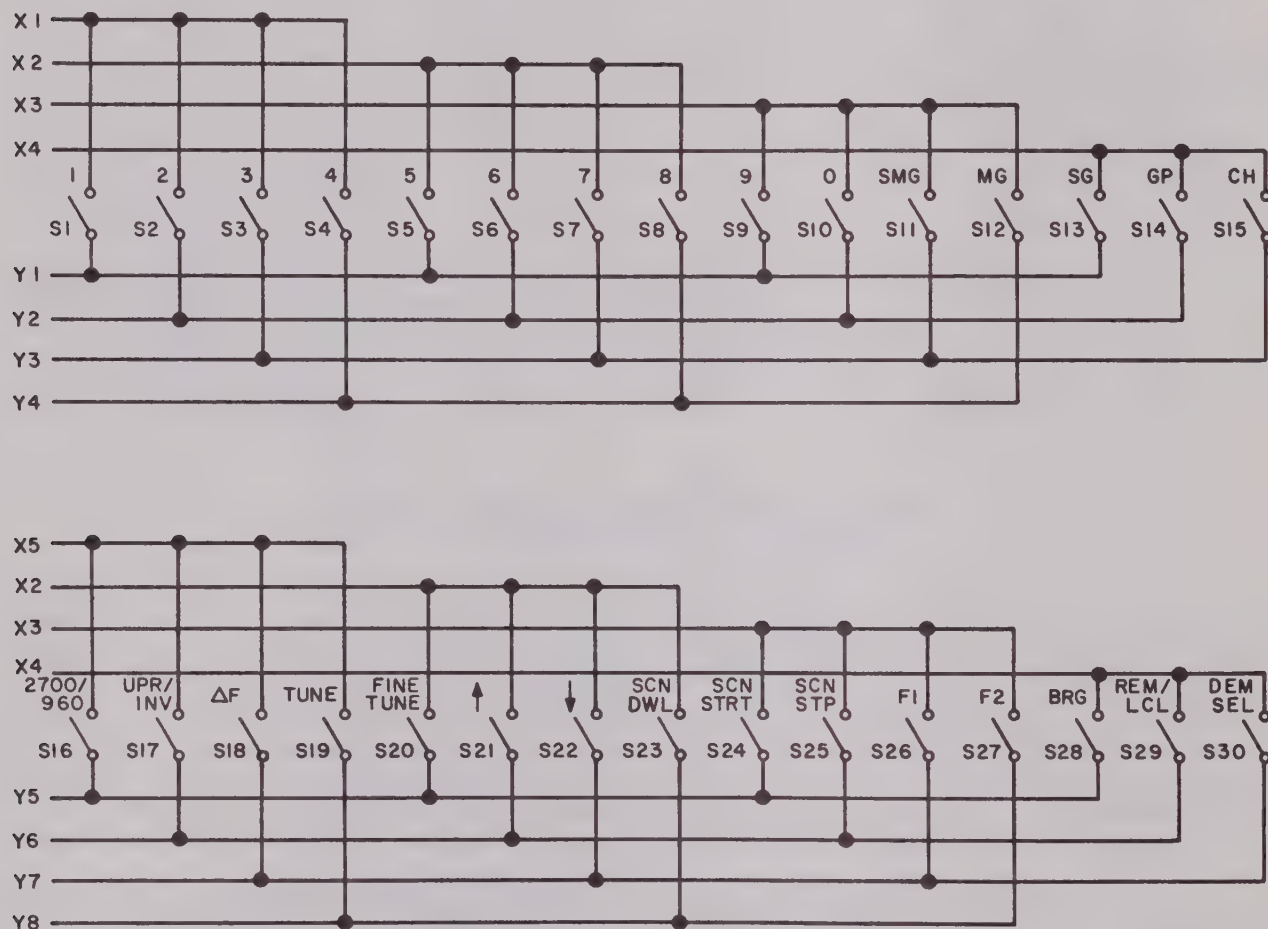


Figure 3-10. Keyboard Switch Diagram

Pressing a key on the Keyboard assembly closes the contacts of a switch (S1-S30). With one of the switches closed, contact is made between an X line and a Y line. With continuity made between the X and Y lines, data is applied to the Digital Motherboard (A9) indicating that a key has been pressed.

The Display Assembly (A1) contains the LEDs utilized to display the demodulator operating parameters. **Figure 3-11** is the block diagram for one-third of the Display assembly.

Display assembly A1 receives display data via the DD0-DD7 lines from the Interface subassembly (A9A3). Data strobes (DST0-DST3) enable display data applied to U2 to be applied to source driver U1 enabling the selected row of LEDs. Data addresses DA0-DA3 applied to decoder U9 enable the selected switch to update the selected column when the data

address enable ($\overline{\text{DAE}}$) line is LOW. This allows displayed front panel displayed data to be updated.

Digital Motherboard assembly A9 contains two keyboard encoders, the three digital subassemblies (Microprocessor A9A1, IEEE-488 Interface A9A2 and Interface A9A3) and filtering for the supply line voltages to each of the three plug-in subassemblies. **Figure 3-1** illustrates the Digital Motherboard and the subassemblies that plug into the Motherboard.

With the three subassemblies inserted into the Digital Motherboard connectors, interconnecting cabling provides for the transfer of data to the Demodulators and front panel Display and also from the Keypad and remote controller.

Control data applied to the Microprocessor subassembly (A9A1) is applied to microprocessor U1. (Refer to **Figure 3-12** for the Microprocessor block diagram.) Data from U1 is applied through latch U2 to the Programmable Read Only Memory (PROM) circuitry (U4-U6) and to Random Access Memory (RAM) U8. Information from memory is applied through U9 or U10 onto the address bus and the data bus. Address information is applied through buffer U9 and onto the address bus. Data is applied through transceiver U10 and onto the data bus. Both bus lines transfer information to the other digital subassemblies. (RAM) U8 stores the current operating parameters. Information is read from (retrieved) memory or written into (stored) as directed by microprocessor U1. Access to PROM, U4-U7 and RAM U8 is accomplished via the data lines (D0-D7) and the address lines (A0-A7). Protection of data stored in RAM U8 is provided via the power up/down circuitry. This circuit provides a battery backup that enables operating parameters stored in U8 to be maintained when power to the unit is turned off or interrupted.

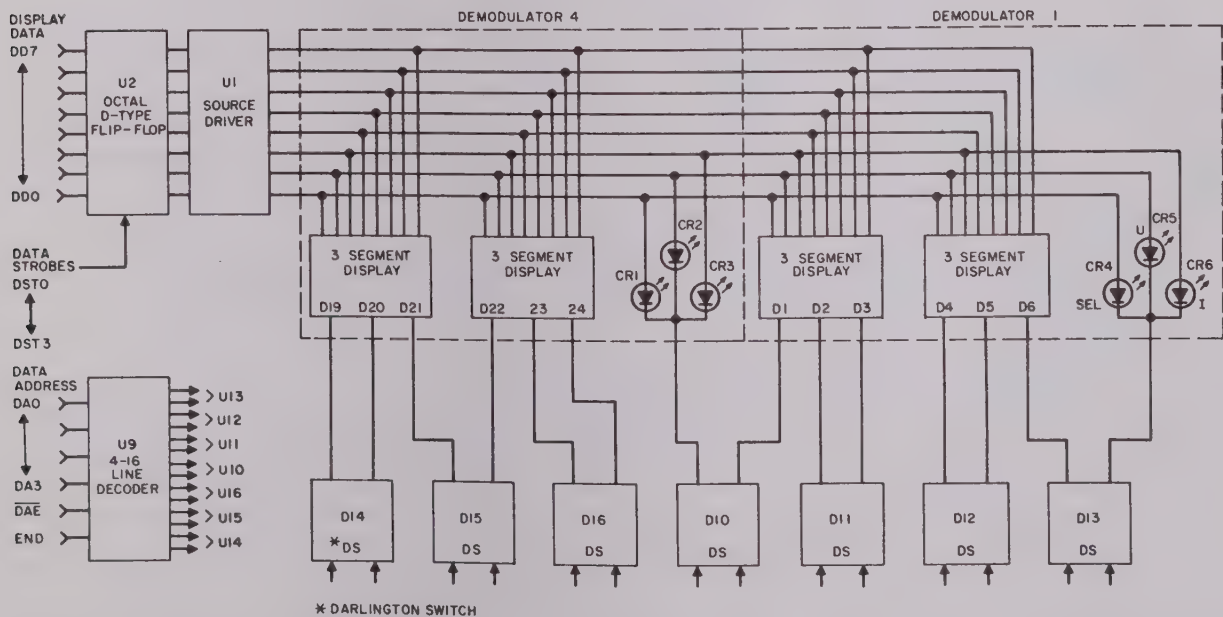


Figure 3-11. Display Block Diagram

IEEE-488 Interface subassembly A9A2 provides the means of exchanging data between a remote controller connected to the rear panel IEEE-488 connector (J1) and the unit. (Refer to **Figure 3-13** for the IEEE-488 Interface block diagram.)

Data is transferred between the remote controller and the microprocessor allowing the unit to be controlled remotely. IEEE-488 multipin connector J1 connects the unit to the BUS. The IEEE-488 BUS is divided into eight data lines (DI01-DI08) and eight control lines. Data signals and control signals are respectively applied through transceivers U1 and U2 to general purpose interface bus (GPIB) U3. GPIB U3 performs the handshake and protocol required to interrelate with the BUS controller and other devices on the BUS. Data transferred by the data lines (D0-D7) is controlled via the register select lines. These register select lines also determine via decoders U8 and U9 whether data from the address switch (S1), through U6 and U4, or the option switch (S2), through U7 and U5, is applied to the data lines and to the Microprocessor subassembly.

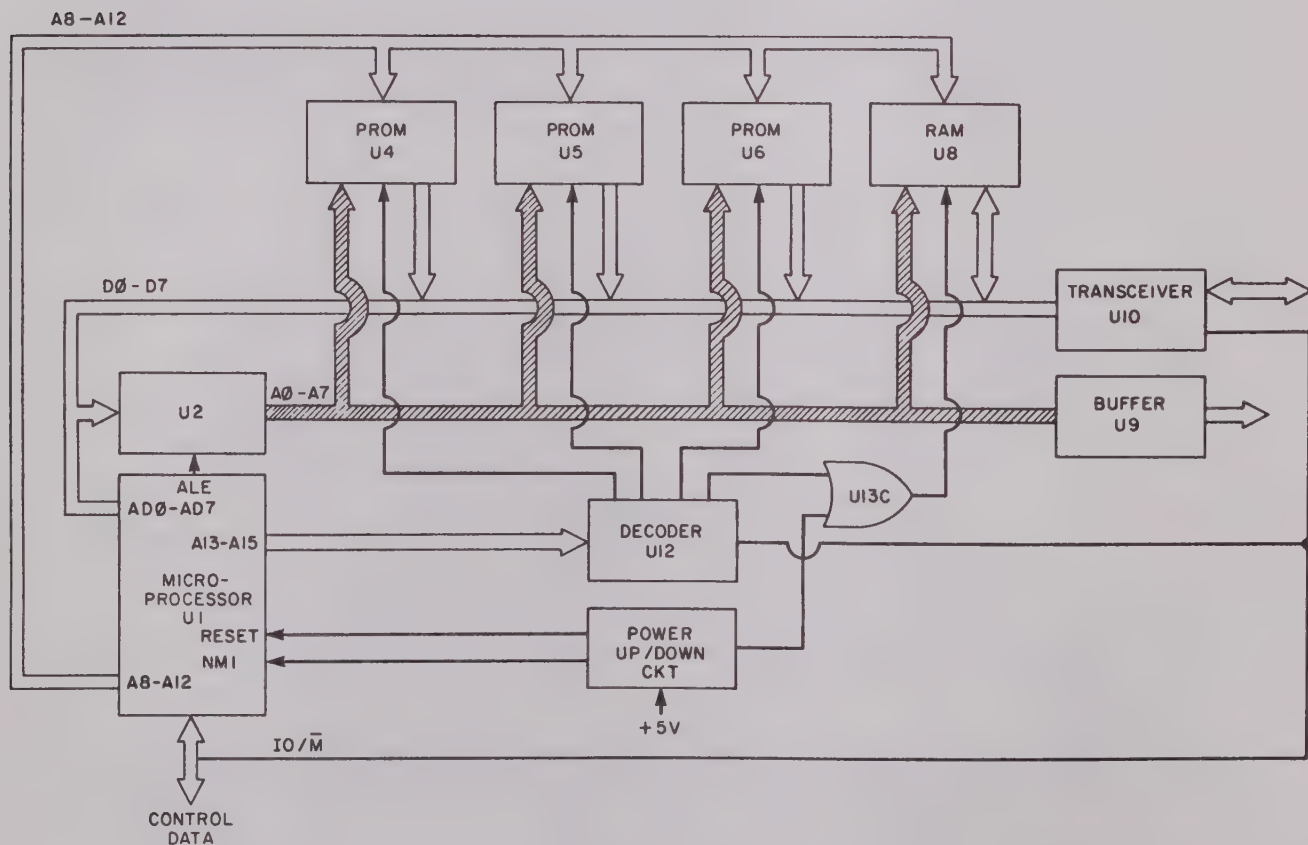


Figure 3-12. Microprocessor Block Diagram

Interface subassembly A9A2 transfers data from the microprocessor (A9A1) and the Display (A1), the Keyboard (A13) and the Demodulators (A3-A8). The Microprocessor (A9A1U1) supplies address data through U12 to U6. Address data and either a read ($\overline{RD}$) or write ($\overline{WR}$) enable are sent to the Interface subassembly, causing U6 to select the parameter or device that is addressed. Refer to **Figure 3-14** for the Interface block diagram.

Data lines D0-D7 transfer the data between the device selected and the microprocessor. These data lines transfer present parameter status to the microprocessor or transfer parameter changes to the device selected.

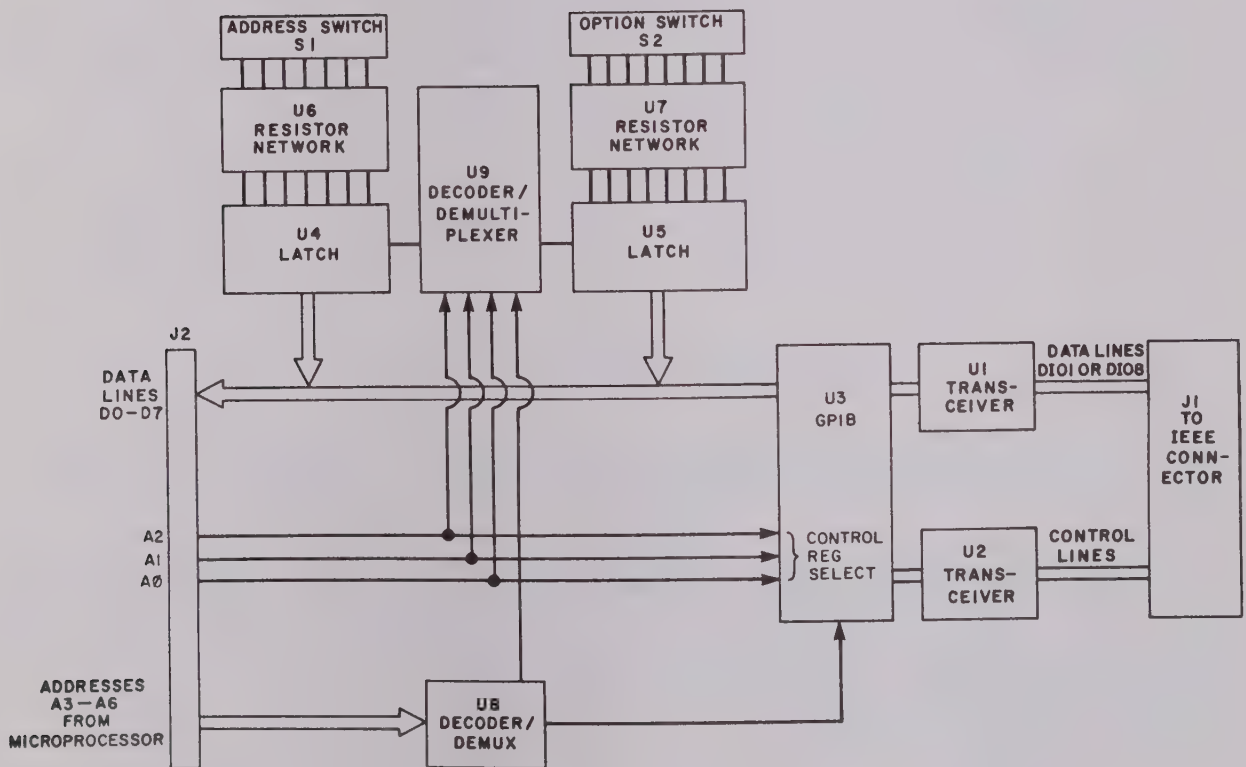


Figure 3-13. IEEE Interface Block Diagram

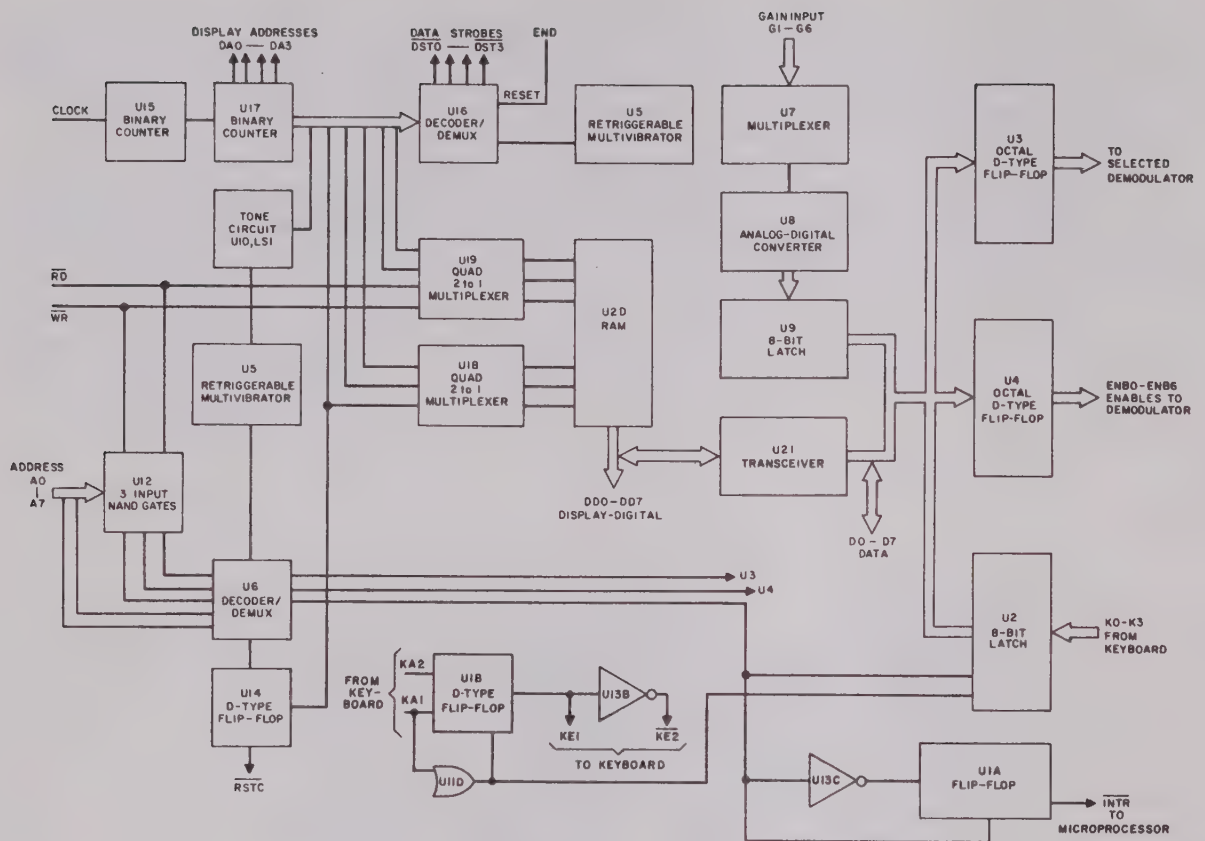


Figure 3-14. Interface Block Diagram

Power Supply assembly A14 rectifies the input line voltages and distributes the supply voltages throughout the unit. **Figure 3-15** is the Power Supply block diagram.

Input line voltages are transformers coupled to the input of Power Supply A14. Two printed circuit boards, A1 and A2 make up the power supply. Input ac voltages are rectified on A1 via CR1 and CR3 and CR2 and CRF and on A2 via U1. Rectified voltages from A1 are applied to voltage regulators U1 and U2 which respectively provide the regulated +15 V and -15 V supply voltages. Rectified voltages from A2 are the +8 V, the +5 V and the +27 V from the DC-DC converter (U3).

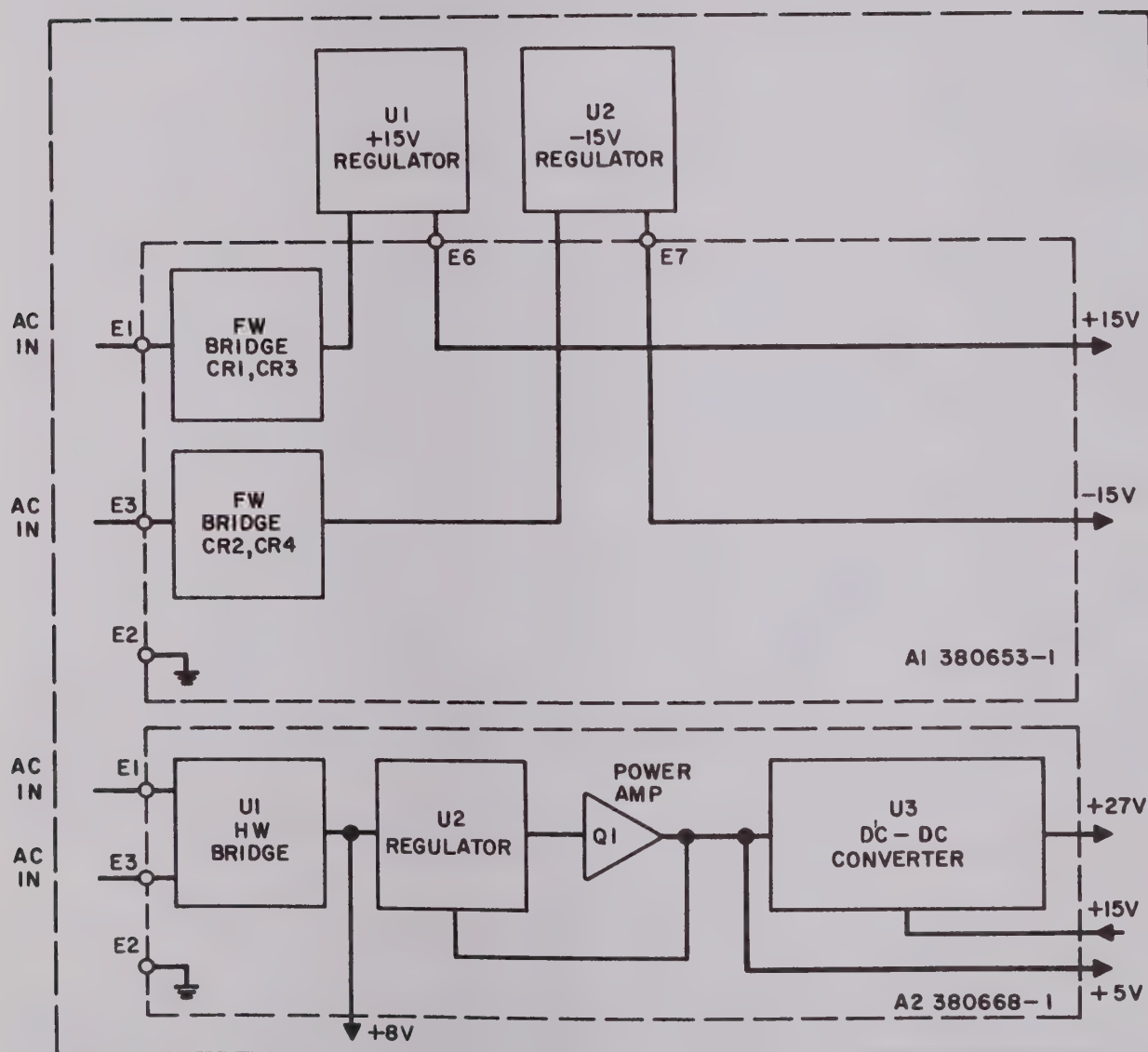


Figure 3-15. Power Supply Block Diagram

3.3 DETAILED CIRCUIT DESCRIPTION

3.3.1 **TYPE 796376-1 REFERENCE GENERATOR (A12)**

The reference designation for this assembly is A12. Refer to **Figure 6-14** for the Type 796376-1 Reference Generator schematic diagram.

Operation of the Reference Generator is dependent upon the setting of the rear panel reference selection switch (S3). In the internal position (INT) +5 Vdc is applied to the crystal oscillator (U1) and frequency divider U1. In the external position (EXT) +5 Vdc is applied to energize transistors Q1 and Q2.

With S3 in the internal position, the 10 MHz ovenized crystal oscillator (U1) has +5 Vdc applied to it through L1. Capacitors C3 and C9 provide filtering of ac variations that may be present on the +5 V supply voltage line.

After a thirty minute warm-up, the output of the ovenized crystal oscillator (U1) is a very stable 10 MHz sine wave. This 10 MHz sine wave is applied to the clock input (pin 11) of frequency divider U1. U1 is a decade counter which divides the 10 MHz output of U1 by 10, producing a 1 MHz output at pin 9. The 1 MHz output from U1 is applied to pins 6 and 10 of multiplexer U2. With U2's select input (pin 1) HIGH, pulses applied to the data inputs. Data is applied to pins 6 and 10 during internal and to pins 5 and 11 during external. This data is coupled to the outputs (pins 7 and 9) and inverted through U3 and U4. 1 MHz output signals at U2 pin 7 are applied to four inputs of hex inverter U4 and output signals at U2 pin 9 are applied to three inputs of hex inverter U3. Outputs from hex inverters U3 and U4 are resistively coupled to output connectors J2-J8.

When switch S3 is in the external position, the +5 Vdc is filtered by C2, C8 and L2. The filtered +5 Vdc is applied to energize transistors Q1 and Q2. With S3 in the external position, the internal ovenized oscillator (U1) is deenergized, and an external 1 MHz, 0 dBm level reference signal is required to be applied at the 1 MHz INPUT (A12J1). The external 1 MHz reference signal is capacitively coupled to the base of transistor amplifier Q1. The amplified output of Q1 is capacitively coupled through C6 to the base of transistor amplifier Q2. The amplified output from Q2 is applied to the data inputs (pins 5 and 11) of multiplexer U2 and as negative feedback, through R7 to the transistor base to provide increased circuit stability.

3.3.2 **TYPE 796370-1 BASEBAND AMPLIFIER (A11)**

The reference designation for this assembly is A11. Refer to **Figure 6-13** for the Type 796370-1 Baseband Amplifier schematic diagram.

An input baseband signal between 300 Hz and 15 MHz with an input level of -25 dBm at the No. 1 BASEBAND INPUT (A11J1) is applied directly to E1 of the Baseband Amplifier printed circuit subassembly (A11A1). The input baseband signals are split into two separate signal paths. One path is applied to relay K1 pin 6. The other signal path is through C1 to the gate of Q1. Signals present at the drain of Q1 are applied to the base of Q2. Output signals at the collector of Q2 are coupled through C4 to the junction of C5 and R7. C5 and R7 couple signals to E3. From E3 the buffered baseband signals are applied to output connector J8

and to Demodulator A3. The buffered output level from the Baseband Amplifier is approximately 5 dB lower than the input baseband level.

Relays K1 through K5 are utilized to bridge the baseband inputs together. When the input baseband signals are jumpered together, via bridging, a single baseband input at A11J1 can simultaneously be applied to all six of the Demodulators. Control of the relays is accomplished digitally via data from the Keyboard applied to E15 and to pin 8 of U3 to control bridging. When the enable line (pin 2) of U3 is HIGH, signals present at the input of U3 are coupled to the output. Other input signals to U3 include the strobe and the clock, applied respectively to pins 1 and 13. These signals are applied to 8-bit shift and store register U1. Input data from E15 is applied to the serial data input (pin 2) of U1. Data input to U1 is entered into the shift register on positive transitions of the input clock. Data in the shift register is transferred to the storage register when the strobe input is HIGH. Connecting the output enable (pin 15) to the +5 Vdc supply line causes data in the storage register to appear at the outputs. This HIGH at the output is applied to the base of the associated transistor (Q3, Q6, Q9, Q12 or Q15) through the base resistor causing the transistor to conduct. When the transistor conducts, the diode between pins 5 and 8, is forward biased causing the relay to energize. Energizing the relay opens the contact between pins 1 and 6 and closes the contact between pins 7 and 3. With the relay energized, the baseband input signal is applied through the relay to the input of the next baseband buffer circuit, thus applying the same input baseband signal to two different Demodulators. Input bridging between any two or more adjacent Demodulators is available to provide the same input signal to several demodulators for processing. As an example; selecting bridging between Demodulator 1 and Demodulator 2 via the front panel keypad inputs applies this digital information through E15 and U3 to U1. Successive HIGHS on the clock and strobe lines output a HIGH on U3 pin 4 causing Q3 to conduct. When Q3 conducts, relay K1 energizes causing the input baseband signal to be applied to the buffer circuit (Q1, Q2 and their associated components) and also through relay K1 to the next buffer circuit. Thus the input baseband signal at J1 is applied to outputs J8 and J9. This provides one input baseband signal to two Demodulator assemblies, or more, if desired. Bridging can be selected between any baseband demodulator input and the next higher numbered Demodulator. Bridging can be selected between Demodulators 1 and 2; 2 and 3; 3 through 6 or 1 through 6 but bridging between 1 and 3 cannot be selected. Bridging is only provided between successive Demodulator assemblies.

BASEBAND INPUT A11J6 couples the baseband signal through C26 to the buffer circuitry and through C30 and R59 to the base of transistor amplifier Q18. The collector output from Q18 is coupled through C31 to the current driver (U2). Output signals from U2 are applied through R67 to provide a 75 Ω output impedance at BASEBAND OUTPUT connector A11J7. This allows a sampling of the baseband signal applied to the input at A11J6.

3.3.3 TYPE 796381-1 DEMODULATOR (A3-A8)

The reference designations for the Demodulator assemblies are A3 through A8. Refer to **Figure 6-3** for the Type 796381-1 Demodulator schematic diagram.

Demodulator assemblies A3-A8 each contain the following subassemblies: Input Converter AXA1, Frequency Converter AXA2, 1st LO Synthesizer AXA3 and 2nd LO Synthesizer AXA4. Refer to **Figure 3-4** for the Demodulator block diagram. Demodulator assemblies A3-A8 receive and demodulate the input baseband signals to provide output audio signals at the headphone jack (J9) and the AUDIO OUTPUT connectors (J10-J15). Demodulator

selection is digitally controlled via the data and control lines from the Interface subassembly (A9A3).

3.3.3.1 Part 380712-1 Input Converter (A3A1-A8A1)

The reference designations for the Input Converters are A3A1-A8A1. Refer to **Figure 6-4** for the Part 380712-1 Input Converter schematic diagram. Input baseband signals between 0 and 15 MHz are applied to the baseband input E1 of the Input Converter subassembly (AXA1). Baseband signals at E1 are attenuated approximately 8 dB by the resistive pad (R1, R2 and R3) and through the low-pass filter (C1-C10 and L1-L3). Filtering the input baseband signal attenuates undesired signals above 17 MHz while passing frequencies between 0 and 15 MHz. Post-filtered signals are attenuated another 3 dB by R4, R5 and R6 before being coupled via JW1 to pins 3 and 7 of mixer U2. The other input frequency at U2 is the 1st LO frequency (25-40.004 MHz). Subassembly AXA3 couples the 1st LO frequency, at a -6.5 dBm level, to P1 of the input converter. First LO frequencies are coupled across C11 to wideband amplifier U1. After amplification the 1st LO frequency is applied to pin 5 of mixer U2 at a level of about +7 dBm. Mixer product frequencies are coupled from U2 pin 4 to the Frequency Converter AXA2 via E2 of the Input Converter and the Frequency Converter subassemblies.

3.3.3.2 Part 380595-1 Frequency Converter (A3A2-A8A2)

The reference designations for the Frequency Converters are A3A2-A8A2. Refer to **Figure 6-5** for the Part 380595-1 Frequency Converter schematic diagram. Sum and difference frequencies from mixer U1 of the Input Converter subassembly (AXA1) are applied to E2 of the Frequency Converter subassembly (AXA2) and to filter FL1. FL1 is a bandpass filter with a 21 kHz bandwidth and 25 MHz center frequency that passes the difference frequencies from mixer U1. These difference frequencies are the 25 MHz 1st IF and are coupled through C1 to amplifier U1. The amplified 1st IF is capacitively coupled to one gate of MOSFET Q1. The other input to Q1 is derived from digital data applied to U12 to control the gain.

Data from the Digital Motherboard (A9) is applied to quad 2-input AND gate U8. Digital information is applied to one of the internal AND gates and the other gate input (pins 2, 6, 9 and 13) are tied together. A HIGH on the enable line at E7 opens the contacts of electronic switch U12 preventing an audio output to the headphone amplifier when the gain is being varied.

With the enable line HIGH, a HIGH at the other input of an AND gate produces a HIGH at the output. Outputs from U8 are applied to U7 (pins 1, 2, and 3) and to the 1st LO (via E16, 17, and 18).

Data at the input of shift-and-store bus register U7 (pin 2) is input into each shift register on positive clock transitions. Data applied to the storage registers appears at the parallel outputs because the output enable is tied HIGH. This data is also available at pin 10 on the negative clock pulse edge. The parallel output data from U7 is sent to U8, to U12 and to digital-to-analog converter U6. Digital-to-analog converter (DAC) U6 reads the input data and produces a proportional negative output voltage (0 to -5 Vdc) at pin 4. The output voltage from DAC U6 is directed to pin 6 of amplifier U2B. Positive voltages at the output of U2B are applied through R6 to the input of U2A and also through R5 and R2, as negative feedback, to the input of U2B. The output from U2A is applied through R15 to pin 2 of amplifier Q1 and

through R11 to the input of U2A as negative feedback. Gain of amplifier Q1 is controlled via the negative voltage from U2A.

From Q1 the 1st IF signal is applied to the parallel resonant tank (L2, C6 and C7). Inductor L2 tunes the tank to 25 MHz. 25 MHz 1st IF signals passed through the parallel resonant tank are attenuated 4 dB via the resistive pad (R19, R20, and R14) and coupled through C10 to wideband amplifier U3. The 1st IF signal is amplified by U3 and coupled through C12 to mixer U4. U4 mixes the 1st IF, at pin 8, with the 2nd LO frequency at pin 1. The 2nd LO Synthesizer (AXA4) applies the 2nd LO frequency (25.5 MHz for the upright mode or 24.5 MHz for the inverted mode) to the Frequency Converter at P1 at a level of -6 dBm. Refer to **Figures 3-16 and 3-17** for the Frequency Converter tuning schemes. The 2nd LO frequency at P1 is coupled to wideband amplifier U5 via C7. U5 amplifies the 2nd LO signal to a level of +8 dBm. The output of U5 is coupled by C13 to pin 1 of mixer U4.

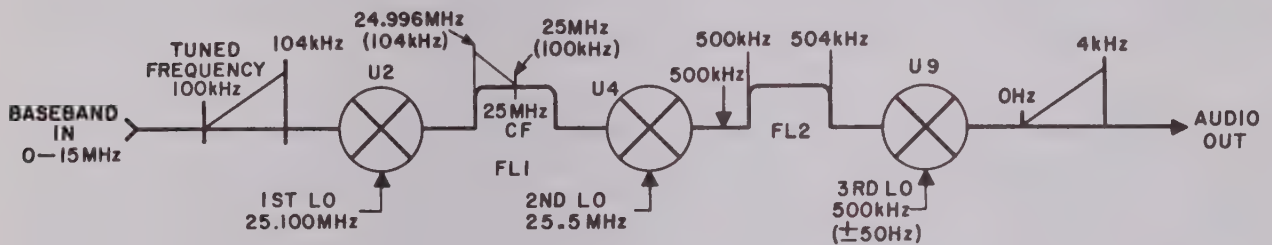


Figure 3-16. Upright Frequency Mode Tuning

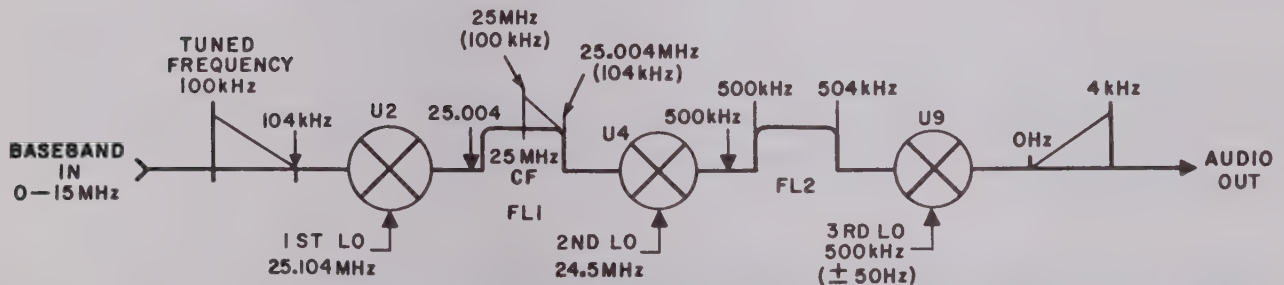


Figure 3-17. Inverted Frequency Mode Tuning

Depending on whether the upright or inverted mode is selected, mixer U4 either up-converts or down-converts to produce a 500 kHz at pins 3 and 7. The 500 kHz 2nd IF is applied through a low-pass filter (L5, C15, and C16) to attenuate undesired higher frequencies. Filtered 2nd IF frequencies are coupled through C18 and R28 to the base of amplifier Q2. Resistors R26-R28, R30 and RT1 establish the biasing for Q1.

Thermistor RT1 provides temperature compensation for amplifier Q2. Temperature compensation of Q2 provides improved gain stability over a wide temperature range.

Amplified 2nd IF frequencies from Q2 are applied to bandpass filter FL2. L7 and R29 match the output impedance of Q2 with the input impedance of FL2. Resistors R31 and R32 match the output impedance of FL2. Bandpass filter FL2 passes frequencies from 500.3 kHz to 503.850 kHz and attenuates all other frequencies, C21 and C25 provide filtering to match FL1. Passband frequencies from FL2 are coupled across C26 to darlington configured amplifiers Q3 and Q4. The output from Q4 is applied via C30 and R63 to the signal input (pin 1) of balanced modulator/demodulator U9. Resistor R63 reduces the level of LO signal.

Zener diode VR1 provides a reduction of the -15 Vdc supply voltage, to -8.2 Vdc, as the negative supply voltage for U9. Capacitors C32 and C33 provide filtering of ac ripple from the -15 V supply voltage line. The 3rd LO frequency (499.950-500.050 kHz) at E15, from the 3rd LO Synthesizer (AXA4) at a level of 100 mV, is coupled by C29 to the carrier input (pin 8) of U9. Gain of modulator/demodulator U9 is controlled by R40 and R41. U9 mixes the 2nd IF frequency with the 3rd LO frequency to produce the sum and difference frequencies at pins U6 and U12. Sum and difference signals at pins 12 and 6 are filtered by C35 and C36 respectively to attenuate the sum frequencies. Resultant audio frequencies (300-3850 Hz) are applied to the inputs (pins 2 and 3) of amplifier U10. U10 is a low noise, balanced amplifier. Negative feedback is supplied back to the input of U10, at pin 2, through R48.

The amplified output from U10 is applied through impedance matching resistor R50 and coupling capacitor C47 to the input of equalizer network U11. This equalizer network serves as the complement to bandpass filter FL2 to reduce the phase error caused by FL2. The phase equalized output from U11 is applied through impedance matching resistor R51 to the low-pass filter (L10, C40 and C41) to eliminate the 500 kHz 3rd LO frequency and its harmonics from the audio output. After filtering, the audio signal is applied through R58 to the non-inverting input of operational amplifier U13. Amplified audio signals from U13 are applied through R61 to E13 as the output audio. Feedback to the input of U13 is provided through R60. Audio output signals at E13 are applied from the Frequency Converter assembly to the rear panel AUDIO OUTPUT connector (J10-J15) for the associated Demodulator assembly.

Output audio signals, in addition to being applied to the rear panel audio connectors (J10-J15), are applied through R52 to the input (pin 4) of electronic switch U12. When the logic level from U7 applies a logic HIGH at U12 pin 2, the interval switch contacts are open and no audio signal is applied to the Headphone Amplifier assembly (A3). Applying a LOW at U12 pin 2 closes the internal switch contacts and provides an audio output at E14 to be supplied to the Headphone Amplifier.

3.3.3.3 Part 380596-1 1st LO Synthesizer (A3A3-A3A8)

The reference designation for this subassembly is A3A3-A8A3 of the Demodulator assembly. Refer to **Figure 6-6** for the Type 380596-1 1st LO Synthesizer schematic diagram.

Two voltage regulators, U1 and U3, supply regulated +5 Vdc and +10.8 Vdc, respectively to the 1st LO subassembly. Regulator U1 supplies +5 V for U2, U3 and U5 and regulator U7 supplies +10.8 V for the oscillator.

The 1 MHz input signal, from J1 is applied to E5 and coupled through C7 to the oscillator input (pin 1) of U2 and is utilized as the reference frequency for the phase lock loop. The serial input phase lock loop frequency synthesizer (U2) internally compares the phase and frequency of the reference signal with the frequency and phase of the variable frequency from

the transmission line oscillator. If a discrepancy is detected between the two signals the phase lock loop to bring the oscillator frequency into synchronization with the reference frequency and phase. Refer to **Table 3-1** for the output response of U2 for the various input conditions. **Figure 3-18** illustrates a typical phase lock loop block diagram.

Table 3-1. Frequency vs. Phase

Condition	ϕ Det A	ϕ Ref	ϕ Var
Var Freq Ref Freq	Neg Pulses	Remains HIGH	Pulses LOW
Ref Freq Var Freq	Pos Pulses	Pulses LOW	Remains HIGH
Var Phase leads Ref Phase	Neg Pulses	Remains HIGH	Pulses LOW
Ref Phase leads Var Phase	Pos Pulses	Pulses LOW	Remains HIGH
Freq and Phase Coincidence	High Z State	HIGH	HIGH

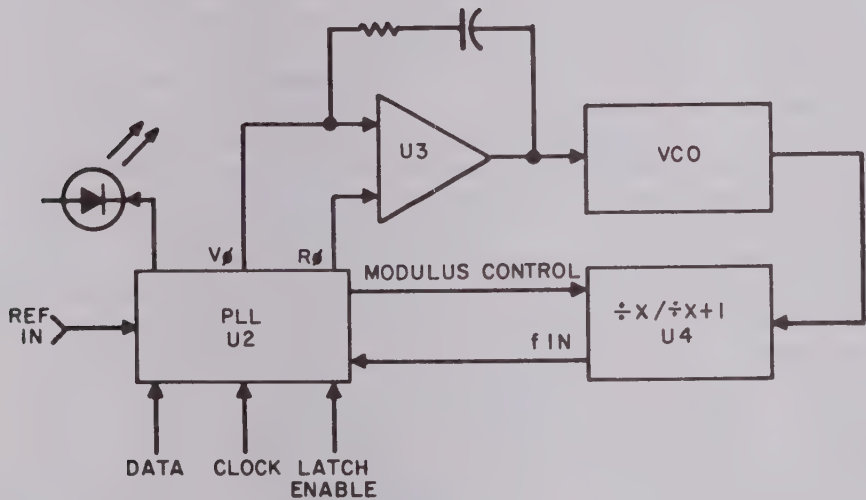


Figure 3-18. PLL VCO Block Diagram

Frequency tuning information is applied to the 1st LO Synthesizer in the form of digital data at E6. This data is applied to the data input line (pin 2) of the shift-and-store bus register (U3). Each time the clock line (E7) varies from LOW to HIGH, data present at pin 2 is entered into U3's internal shift registers. When the strobe line, from E8, is HIGH, the data in each shift register is transferred to the storage register. Connecting the output enable line (pin 15) to the +5 V supply voltage line causes data that is entered into the storage register to appear at the outputs (pins 4, 5 and 9). The logic level at pin 4 determines whether the high band (a HIGH) or the low band (a LOW) is selected. The 1st LO divide ratio is determined by the logic level at pin 5. When the level at pin 5 is HIGH, Q3, Q4 and U9 provide a divide by 10 ratio. When the level at pin 5 is LOW, Q3, Q4 and U9 provide a divide by ratio of 8. This change in the 1st LO divide ratio coincides with a similar change in the synthesizer divide ratio. A reference divide by of 100 is provided when U18 ($\div 10$) is selected, producing divided down reference and variable frequencies of 10 kHz. A reference divide ratio of 125 is provided when frequency divider U9 ($\div 8$) is selected. This produces internal reference and variable frequencies of 8 kHz.

Frequency data input at E6 is applied to U3 pin 2 providing the means of tuning the 1st LO Synthesizer, in 1 kHz steps, from 25 MHz to 40.004 MHz. Two frequency bands are utilized (low band with a $\div 10$ ratio or high band with a $\div 8$ ratio) by the phase lock loop providing a 1 kHz tuning resolution across the synthesizer tuning range. Band selection is accomplished by the logic level at U3 pin 4. A LOW at pin 4 selects the low band and a logic HIGH selects the high band. Selecting the low band causes the inverted output of operational amplifier U10 to forward bias CR13 and CR14 thus adding capacitors C50 through C53 into the oscillator circuit to decrease the oscillator frequency.

U3's serial output, pin 9, couples tuning data to the phase lock loop frequency synthesizer (U2). This tuning data is input to U3 when the clock input to U36 (pin 3) and U2 (pin 9) is HIGH, U3's output data is U2's data input, at U2 pin 10 and is applied to its internal shift registers. Depending on the last data bit entered, the data is entered into either the reference counter register (last data bit HIGH) or the $\div N$ and $\div A$ counter registers (last data bit LOW) in U2. Each LOW to HIGH transition of the clock input (pin 9) shifts one bit of data into the selected shift register(s). (Refer to **Figure 3-19** for the block diagram of the serial input phase lock loop frequency synthesizer.) A HIGH on the latch enable line (pin 11) shifts the data in the shift register into the selected latch(es) and into the associated divide by counter(s). When the data is loaded into the divide by counter(s), the two frequency inputs (the reference frequency at pin 1 and the variable frequency at pin 8) cause their associated counters to count down. The counter outputs are applied to a single output phase detector. At the single output phase detector, the frequency and phase of both input signals are compared. Any difference in frequency and/or phase causes the phase detector to generate a loop error signal. This error signal is applied to the double ended phase detector. These two outputs, pins 15 and 16, are applied to the inputs of operational amplifier U4. (Refer to **Table 3-1** for the output responses for the various input conditions.) U4 amplifies the input error signal and applies it through C14 and R10 back to the input, as negative feedback, and through impedance matcher R13 and RF choke L2 to the variable capacitance diodes used to tune the frequency of the transmission line oscillator.

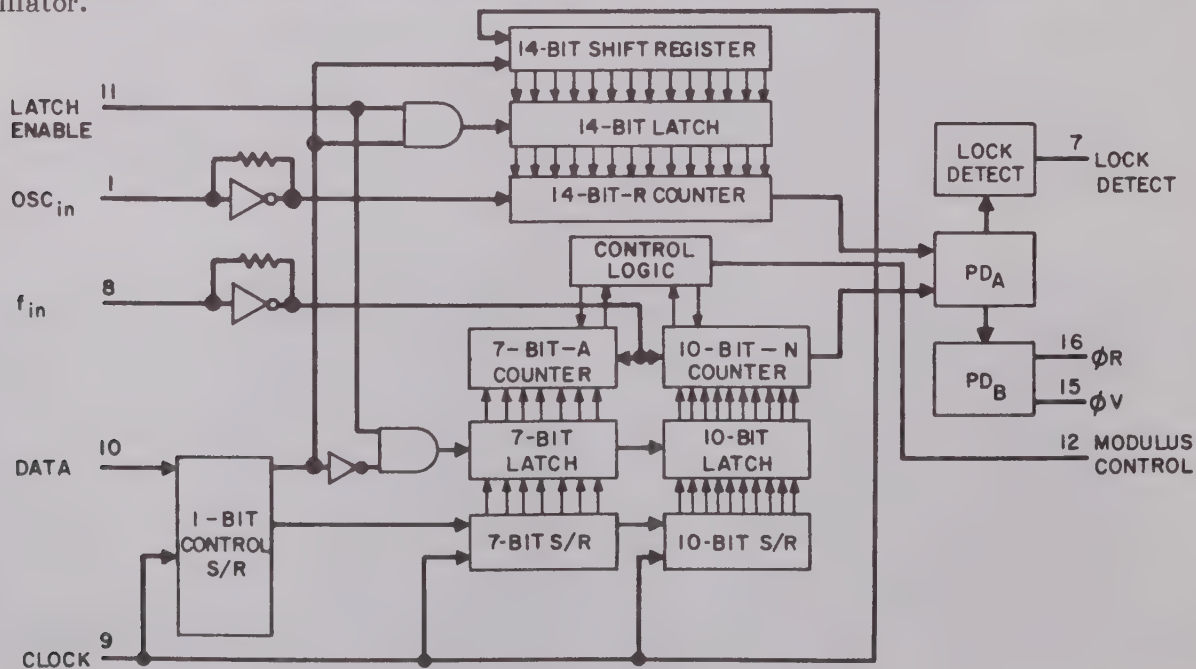


Figure 3-19. PLL Synthesizer Block Diagram

Voltage regulator U7 supplies a regulated +10.8 Vdc to the transmission line oscillator circuitry to bias the oscillator (Q1). The oscillator frequency is varied by the value of capacitance attached to the transmission line. As the value of capacitance increases the transmission line oscillator frequency decreases. Likewise, when the capacitance on the transmission line decreases, the oscillator frequency increases. The low-band oscillator frequency range is from 250 MHz to 320 MHz. At these frequencies the capacitance at one end of the transmission line is appears as an inductor on the opposite end of the transmission line.

Phase lock loop operation is best understood when an unlock condition exists, like tuning the 1st LO. Changing the input frequency data to the 1st LO Synthesizer causes the data entered into the phase lock loop frequency synthesizer (U2), through shift and store bus register U3 to produce a different starting frequency for the counters. Changing the frequency data causes the phase lock loop to momentarily unlock. Unlocking of the phase lock loop (PLL) is caused when the $\div R$ (reference) and the $\div A$ and $\div N$ (variable) counter outputs are not identical, as compared by the single output phase detector. A difference in frequency and/or phase causes the single output phase detector to produce a loop error signal. This loop error signal is applied to the double output phase detector which produces output pulses to the input of operational amplifier U4. U4 amplifies the error signal and applies the error voltage to the variable capacitance (varicap) diodes CR1 through CR12 to vary the frequency of the transmission line oscillator. Capacitors C26 and C27 on one end of the transmission line are converted to an inductor on the other end of the transmission line. This converted inductor value and the capacitance of the varicap diodes (CR1-CR6) form a LC tank for transistor oscillator Q1. The resonant frequency of the LC tank depends on the values of inductance and capacitance. As the value of either the inductor or the capacitor increases the oscillator frequency decreases. The transmission line oscillator output frequency is coupled through C4 to the junction between the 3 dB attenuator pad (R15, R16 and R17), the $\div 10$ counter (U8) and the $\div 8$ counter (U9). One signal path is through the attenuator pad and through C19 to the input of the programmable divider (U5). Dependent upon the control line (pin 1) logic level, the divide ratio is either 80 (the control line HIGH) or 81 (the control line LOW). The modulus control line (U2 pin 12) logic level is controlled by the data entered into $\div N$ and $\div A$ counters. At the beginning of the frequency synthesizer phase lock loop count cycle, the modulus control line is LOW and U5 divides by 81. When the $\div A$ counter counts down to zero, the modulus control line goes HIGH and remains at that level until U5 counts down to zero and then divides by 80 for the remaining count in the $\div N$ counter. This divided down transmission line oscillator frequency is coupled from divider U5 through capacitor C11 to the variable frequency input (pin 8) to U2. The single output phase detector compares the divided down reference and variable frequencies for synchronization. When both the reference and variable frequencies are identical in frequency and phase, a lock condition exists and the single output phase detector no longer produces a loop error signal. With no error signal to drive the double output phase detector, the reference (R $\emptyset$) and variable (V $\emptyset$) outputs are only narrow synchronized spikes. Also the lock detect line (pin 7) goes LOW. When an unlock condition exists and the frequency synthesized phase lock loop is unable to tune the transmission line oscillator frequency to the same frequency as the reference frequency, the lock detect line goes HIGH. A HIGH at pin 7 causes the DSI LED to illuminate, giving a visual indication that the phase lock loop is unlocked.

In addition to being applied through U5 to the frequency synthesizer (U2), the oscillator signal is also applied to the inputs of two frequency dividers U8 and U9. Oscillator signals are coupled through C23 to the clock input (pin 12) of frequency divider U8 and directly to the clock input (pin 1) of frequency divider U9. U8 divides the oscillator frequency by 10 and U9 divides the oscillator frequency by 8. Frequency divider selection is accomplished via the logic level of U3 pin 5. With a HIGH at U3 pin 5, Q3 is reverse biased and transistor Q2 is biased to conduct, allowing U8 to divide the input oscillator frequency by 10. A LOW

at U3 pin 5 reverse biases Q2 and transistor Q3 conducts. When Q3 conducts, its output causes transistor Q4 to conduct allowing the oscillator frequency to be divided by 8 and applied to the output (pin 8).

Output frequencies from U8 are coupled through C35 and R32 output frequencies from U9 and coupled through C36 and R34 and the input of the bandpass filter. The bandpass filter (C45, C46, C47, L6 and L7) passes the 1st LO frequencies (25 MHz-40.004 MHz) and attenuates frequencies outside of the passband. This filter provides attenuation of oscillator harmonics above 41 MHz. Frequencies within the passband are not attenuated and are coupled through capacitor C48 to the input of U6. U6 is a wideband amplifier that amplifies the 1st LO frequencies to a level of about -6.5 dBm. First LO frequencies, 25 MHz-40.004 MHz, are coupled through C56 and E10 to connector J2.

3.3.3.4 Part 380544-1 2nd LO Synthesizer (A3A4-A8A4)

The reference designation for this subassembly is A3A4-A8A4. Refer to **Figure 6-7** for the Type 380544-1 2nd LO Synthesizer schematic diagram.

Two voltage regulators, U1 and U6, provide independent and regulated supply voltages for the frequency synthesizer (U2) and the transmission line oscillator. Voltage regulator U1 supplies a regulated +5 Vdc to the frequency synthesizer (U2). Voltage regulator U6 supplies a regulated +10.8 Vdc to power the transmission line oscillator circuitry.

The phase lock loop frequency synthesizer (U2) receives a 1 MHz reference signal from the Reference Generator assembly (A12). (Refer to **Figure 3-10** for the block diagram of U2.) This 1 MHz reference signal is applied through J2 to E1 of the 2nd LO Synthesizer subassembly (A3). From E1 the reference signal is capacitively coupled through C1 to the oscillator input (pin 1) of serial input phase lock loop (PLL) synthesizer U2. The oscillator input signal is applied to an internal ÷R counter with a fixed divide ratio of 10. Thus, the 1 MHz reference signal after being divided by 20 becomes 50 kHz and is applied as one of the inputs of the internal single output phase detector. Frequency information from the frequency converter assembly (A1) is applied to E3 in the form of binary data and is applied to the data input (pin 10) of U2. Each time the clock line (pin 9) level changes from a LOW to a HIGH level, the data bit at pin 10 is shifted into the internal shift registers. If the last data bit entered is HIGH, the reference counter latch is selected and if the last bit is LOW, the ÷N and ÷A latches are selected. When the latch enable input (pin 11) is HIGH, the data is latched from the shift register into the reference divider (÷R) and if the last data control bit is LOW, then the ÷N and ÷A registers are selected. Data entered into the ÷N and the ÷A registers form the variable output which is the other input to the single output phase detector. The single output phase detector compares the frequency and the phase of both the reference frequency (pin 1) and the variable frequency (pin 8). This phase detector produces a loop error signal, in the form of pulses, when either the frequency and/or phase of the reference and variable frequencies are not synchronized. Error signals are applied to a two output phase detector. The double ended phase detector outputs are the variable phase (pin 15) and the reference phase (pin 16). Refer to **Table 3-1** for the various frequency/phase differences and the corresponding signal response. Detected differences in frequency or phase produce an output loop error signal, from pin 15 or 16, which is applied to the input of operational amplifier U3. The reference phase output is applied through R4 and R5 to the inverting input (pin 2) and the variable phase output is applied through R6 and R7, to the noninverting input (pin 3) of U3. U3 amplifies any differences between the two input signals. This amplified difference signal is applied through R11, L1 and filtered before being applied to the transmission line oscillator circuitry. Negative feedback is

supplied through C8 and R8 back to the input of U3. Inductor L1 and the filter, composed of C15, R12 and C16, remove noise from the tuning voltage line. The filtered output tuning voltage is applied through R13 to the transmission line oscillator circuit.

The transmission line oscillator circuitry consists of transmission line Z1, oscillator Q1, tuning diodes CR1-CR6, voltage regulator U6, RF choke L3 and regulator filters C26 and C27. The oscillator (Q1) oscillates at a frequency determined by the value of capacitance connected to the transmission line (Z1). This oscillator frequency is either 245 MHz or 255 MHz. The transmission line utilized is approximately one eighth of a wavelength at the oscillator frequencies. The transmission line is utilized as a reactance transformer to change a capacitive reactance connected on one end of the transmission line into an inductive reactance at the other end of the line. This provides the means for producing a high Q inductor by terminating the transmission line with a high Q capacitor.

The transmission line oscillator frequency is dependent upon the digital data applied to the phase lock loop (PLL) synthesizer (U2). When locked on frequency the oscillator frequency is either 245 MHz for the Inverted mode or 255 MHz for the Upright mode. Changing the 2nd LO synthesizer tuned frequency causes the PLL synthesizer to output an error loop signal to the input of operational amplifier U3. U3 amplifies this loop error signal and couples it through impedance matching resistor R11 and also through C8 and R8 as negative feedback to the amplifier input. The loop error signal is coupled through RF choke L1 and through the tuning voltage filter (C15, R12 and C16). This error signal tuning voltage is applied to the variable capacitance tuning diodes (CR1-CR6). As the tuning voltage increases (reverse bias voltage) the diode capacitance decreases and the oscillator frequency increases. Decreasing the tuning voltage causes the diode capacitance to increase causing the oscillator frequency to decrease.

Capacitor C17 blocks the dc voltage from the voltage regulator U6. U6 supplies a regulated 10.8 Vdc supply voltage for the oscillator circuitry. This supply voltage is applied through R20 to a dual purpose filter network of L3, C26 and C27 that filters the line voltage and also terminates one end of the transmission line. Capacitors C23, C24 and C25 act as a high Q inductor for the oscillator circuit. Resistor R19 provides biasing for Q1 and C18 provides the feedback path for the oscillator tank (L2 and C18). Oscillator frequencies are coupled through L6 and split before being applied through C31 to frequency divider U5 and through R17 and C14 before being applied to frequency divider U8. Programmable frequency divider U4 divides the oscillator frequency by either 80 or 81, depending on the status of the control input line (pin 1). When the control input line is LOW, U4's divide ratio is 81. When the control input is HIGH, the divide ratio is 80. Phase lock loop synthesizer U2 controls the status of the control input line to produce a divide ratio that results in a 50 kHz output frequency from U4. This 50 kHz signal is applied to the f_{in} (pin 8) of U2 as the variable frequency input. When both of the frequency inputs to U2 are synchronized, the synthesizer phase lock loop is locked. If either frequency varies, the phase lock loop tunes the oscillator to bring its variable frequency into synchronization with the reference frequency. If the phase lock loop is unable to tune the oscillator frequency far enough to produce a lock condition, the normally HIGH lock detect output (pin 7) strobes LOW, forward biasing DSI and causes it to blink at a rate proportional to the error in frequency. The lock detect line is held LOW, illuminating DSI, if the phase lock loop is unable to achieve a lock.

Frequency divider U5 divides the transmission line oscillator frequency by 10 to produce the 2nd LO synthesized frequency of either 24.5 MHz for the Inverted mode or 25.5 MHz for the Upright mode. This oscillator frequency (24.5 MHz or 25.5 MHz) is coupled by C43 and through the resistive pad (R24 and R16) to reduce the signal level before being filtered. Capacitors C34, C35 and C36 and inductors L4 and L5 form a low-pass filter to

attenuate the harmonics of the 24.5 or 25.5 MHz. After filtering, the synthesized frequency is coupled across C37 to operational amplifier U7. The signal is amplified by U7 and capacitively coupled to the second harmonic attenuator (C44, L8 and C45) before being applied to J1. The signal at J1 is the 2nd LO synthesized frequency of either 24.5 or 25.5 MHz at a level of approximately -4.3 dBm.

3.3.4 TYPE 776009-1 3RD LO SYNTHESIZER (A10)

The reference designation for this assembly is A10. Refer to **Figure 6-12** for the Type 796376-1 3rd LO Synthesizer schematic diagram.

A 1 MHz reference signal is applied to connector J1 of the 3rd LO Synthesizer subassembly and is directly coupled to E1 of the 3rd LO Synthesizer printed circuit (PC) assembly (A10A1). The 1 MHz reference signal is capacitively coupled across C2 to the input of the phase lock loop frequency synthesizer (U2). Voltage regulator U1 supplies a regulated +5 Vdc to pin 4 of U2. C3 removes ac variations that may be on the voltage supply line. The phase lock loop frequency synthesizer is connected to operate in the external reference mode. In the external reference mode, the 1 MHz signal is applied to an internal 14 bit reference counter that is set to a constant $\div 5000$ ratio. Dividing the 1 MHz reference frequency by 5000 produces a 200 Hz signal that is fed, as the reference, to one input of an internal phase detector. The other input to the phase detector comes from the amplified and divided 10 MHz crystal oscillator Y1. This phase detector compares both 200 Hz input signals (one called the reference and the other called the variable) to determine whether their frequency and/or phase are the same. If either the frequency and/or the phase of the 200 Hz reference and variable signals are not identical, the phase detector produces an error signal. When the variable frequency is greater than the reference frequency or the variable frequency phase leads the reference frequency phase, the phase detector produces negative pulses. When the variable frequency is less than the reference frequency or the phase of the variable frequency lags the reference frequency phase, the phase detector output is positive pulses. When the variable frequency is equal to the reference frequency and both phases are the same, the phase detector produces a high impedance state and extremely narrow spikes indicating a "locked" condition. (Refer to **Table 3-1** for the frequency/phase responses.) Any other condition than a locked condition produces an error signal that is applied to U2's double ended phase detector. The outputs of this double ended phase detector are pulses at either pin 15 (variable phase output) or pin 16 (reference phase output). The output reference error signal is resistively coupled through R4 and R5 to the inverting input of operational amplifier U3. Capacitor C5 provides filtering of positive spikes on the reference phase line. Likewise, the variable phase output signal is resistively coupled through resistors R6 and R7. C6 provides filtering of spikes on the variable phase line before being applied to the noninverting input of U3. Any difference between the input signal levels of U3 is greatly amplified at the operational amplifier output. Changes in the amplifier output are coupled across C7 and through R8 to provide a negative feedback path to the input of U3. Output voltages from U3 are applied through resistor R10 and filtered by C14 before being applied to the oscillator circuitry (R11, CR1-CR4, C16, Y1 and R16). Diodes CR1 through CR4 are variable capacitance diodes used to vary the oscillator frequency. As the amplifier output voltage increases, the diode capacitance decreases and the oscillator frequency increases. When the amplifier output voltage decreases, the diode variable capacitance increases and the oscillator frequency decreases. The oscillator output signal is applied to the high input impedance base of transistor Q1. Q1's output is coupled through R17, reduced by C19 and C20 and applied back to its base. Q1's output is also applied to the base of transistor Q3. The output of Q3 is coupled through C2 to the base of transistor amplifier Q2.

The output signal from Q2 is applied to frequency dividers U5 and U4 with negative feedback provided through R20 to the base of Q2. The amplified oscillator signal is split and applied to both of the frequency dividers (U4 and U5). U5 divides the input 10 MHz oscillator frequency (at pin 4) by 20, producing a 500 kHz signal at the output (pin 13) that is applied to the inputs of the hex buffer/converter (U6). Each output from U6 is attenuated by a 6 dB resistive pad producing an output level of approximately 100 mV that is applied to each Demodulator (A3-A8) as the 500 kHz (± 50 Hz) 3rd LO frequency.

The other path for the 10 MHz oscillator signal is through R13 and C13 to the input (pin 5) of the programmable divider (U4). U4 divides the 10 MHz signal by either 80 or 81. The divide by ratio of U4 is controlled by the modulus control line from the phase lock loop synthesizer (U2). When the modulus control output level (pin 12) is LOW, U4 divides by 81. When the modulus control output is HIGH, U4 divides by 80. This divided oscillator frequency is coupled by C11 to U2's input frequency (pin 8) and to its two variable counters ($\div A$ and $\div N$). At the beginning of the count sequence, the modulus control line is LOW causing U4 to divide by 81. When the synthesizer's $\div A$ counter counts down to zero, the modulus control line goes and remains HIGH until the $\div N$ counter counts down to zero.

At the beginning of the count cycle both the $\div N$ and the $\div A$ counters are counting down from their preset values. The $\div A$ counter always counts down to zero prior to the $\div N$ counter. Data is loaded into the $\div N$ and $\div A$ registers, presetting them, via the data (pin 10) and clock (pin 9) pins of U2. When the latch enable (pin 11) is HIGH data is latched into the internal registers. Each clock line LOW to HIGH logic transition causes one data bit on the data line to be entered into the internal registers. If the last data bit entered is HIGH, the reference counter latch ($\div R$) is selected and if the last data bit is LOW the variable counter latches ($\div N$ and $\div A$) are selected. Tuning the 3rd LO is accomplished via changing the data loaded into the internal registers of U2 which also changes the divide ratio of the shift registers ($\div N$ and $\div A$). A 5 Hz increase in the demodulator tuned frequency causes the data line to input data into the shift registers of U2. When the latch enable is HIGH data is latched from the shift register into the $\div N$ register and U2 changes the divide ratio of U4 to tune the 3rd LO frequency by 5 Hertz.

When the tuned frequency is different from the oscillator frequency, the phase detector in U2 generates a negatively pulsed loop error signal. This error signal drives the variable phase line LOW and is applied to the noninverting input of amplifier U3. The amplified error voltage is applied to the variable capacitance diodes causing the oscillator frequency to increase. The increased oscillator frequency is divided and applied through the buffer U6 to each Demodulator (A3-A8). Completing the phase lock loop, the divided oscillator frequency is applied to the $\div N$ and $\div A$ registers whose output is applied to the phase detector eliminating the negative loop error signal.

When an unlock condition exists, U2's lock detect output (pin 7) is pulsed LOW. This forward biases the LED causing it to illuminate. When the phase lock loop is locked, the lock detect output is HIGH and the LED is extinguished.

3.3.5 TYPE 796387-1 HEADPHONE AMPLIFIER (A2)

The reference designation for this assembly is A2. Refer to **Figure 6-2** for the Type 796387-1 Headphone Amplifier schematic diagram.

The Headphone Amplifier provides a sample audio signal for the Demodulator under front panel control. The audio signal is coupled through C12, of the Demodulator under control of the front panel, to input (E1) and the resistive divider (R1 and R2). The audio signal is coupled through C1 to the input of amplifier U1. Gain of U1 is adjustable via the front panel PHONE LEVEL control knob (R8). The output audio signal from U1 is capacitively coupled through C4. R4 attenuates the audio signal before being applied to the input of amplifier U2. The output of U2 is resistively coupled through R8 to the output (E5) of the Headphone Amplifier and through R7 to the input of U2. This audio signal is LC filtered by L1 and C5 to the front panel phone jack (J9) to providing a 600 ohm sample of the demodulated audio signal.

Capacitors C2, C5 and C6 provide filtering of ac variations which may be riding on the dc voltage lines, thus shorting the ac variations to ground.

3.3.6 TYPE 796380-1 KEYBOARD ASSEMBLY (A13)

The reference designation for this assembly is A13. Refer to **Figure 6-15** for the Type 796380-1 Keyboard assembly schematic diagram.

The Keyboard is composed of thirty, normally open pushbuttons. These Keyboard pushbuttons control all of the unit operating parameters, except GAIN and HEADPHONE levels, during local control. Depressing a pushbutton key on the Keyboard closes the contacts for the selected function. When the switch contacts are closed, a signal path is completed between the X contact on one side of the switch and the Y contact on the other side of the switch. If, for example, S1 is depressed and the X1 input is scanned by the 16 key encoder (U1) of the Digital Motherboard, X1 goes LOW and Y1 goes LOW. This causes the interface counter to be disabled and keeps the X1 line LOW. When Y1 is LOW, the key bounce circuit timing of U1 is initiated, locking out the other Y inputs. Once the key-bounce circuit times out, the input data to U1 or U2 of the Digital Motherboard is latched to the data output and the data available (pin 12) goes HIGH. Releasing the key causes the data available output to go LOW and initiates the debounce circuit timing. After the debounce circuit has timed out, another key may be depressed. The output latches are set to a high impedance state when the output enable is LOW. Output data from the 16 key encoders is applied to J3 of the Interface subassembly (A9A3).

3.3.7 TYPE 796374-1 DISPLAY BOARD (A1)

The reference designation for this assembly is A1. Refer to **Figure 6-1** for the Type 796374-1 Display Board schematic diagram.

The Display Board contains the single and 7-segment LEDs utilized to display the unit operating parameters for the Demodulator. Information displayed via the Display Board includes: selected demodulator, tuned frequency, mode (upright or inverted), fine tune offset or the scan dwell time, bridging, control (local or remote), CCITT plan (2700 or 960 channels), and scan enable. These LED displays combine to provide the unit operating conditions at a glance.

Display data lines DD0-DD7 applied to the Display Board (pins 26-31) from the Interface subassembly (A9A2) apply display data to the 4 parallel octal D-type flip-flops (U2-U7). Valid display data applied to the D inputs are transferred to their associated Q outputs on positive going transitions of the clock pulse (pin 11). Each flip-flop's clock line is controlled by a separate display strobe from the Interface subassembly (A9A3). A LOW on the display strobe 0 line (pin 36) has no effect on U2. When the DST0 line goes HIGH, the data

applied to the inputs is transferred to the outputs of U2. Data on the outputs of U2 is applied directly to the inputs of U3. U3 is a high voltage, high current, source driver used to drive the LEDs of Demodulator 4 and Demodulator 1 through current limiting resistors R1-R8. Only one of the two Demodulator's LEDs receive the display data at a time. Selection of the demodulator display to be updated is accomplished via the display address (DA0-DA3) logic levels. Display address logic levels are applied to the inputs of U9. When the display address enable of U9 (pin 23) is LOW, address data applied to the inputs is latched to the outputs. U9 decodes the 4 data input lines to 14 output lines. The selected output line goes HIGH when it is selected. The selected HIGH output is applied to the base of the corresponding darlington switch (U11-U16). Utilizing the different data address combinations allows one-half of the darlington switch to conduct or both halves of the switch to conduct. These darlington switches supply the current necessary to drive the LEDs. **Table 3-2** indicates the input data address required to select the associated LED columns.

Table 3-2. U9 Data Address Output Selection

Data Address A B C D	Selected Output	Pin Number
0 0 0 0	S0	11
1 0 0 0	S1	9
0 1 0 0	S2	10
1 1 0 0	S3	8
0 0 1 0	S4	7
1 0 1 0	S5	6
0 1 1 0	S6	5
1 1 1 0	S7	4
0 0 0 1	S8	18
1 0 0 1	S9	17
0 1 0 1	S10	20
1 1 0 1	S11	19
0 0 1 1	S12	14
1 0 1 1	S13	13
0 1 1 1	S14	16

NOTE

The selected output is HIGH as long as the $\overline{\text{DAE}}$ line (pin 23) is LOW. When the $\overline{\text{DAE}}$ line is HIGH, all selected outputs are LOW.

Thus to update the front panel display, three sequential events must occur. First, display data must be applied to the DD0-DD7 lines. These display data lines apply the information to the four parallel octal, D-type flip-flop inputs. With the output enable LOW, the input data is applied to the outputs. Second, a data strobe (DST0-DST3) line requires a LOW to HIGH transition to enable one of the four octal flip-flops (U2, U4, U6, and U7) to output the received display data to the inputs of the display drivers (U1, U3, U5, and U8). Each source driver produces a high voltage, high current through a current limiting resistor to the entire row of LEDs. Third, this data applied to one particular row of LEDs is input to the LEDs. Using the

data select lines (DA0-DA3) one column at a time is selected. This allows one LED display at a time, either a 7 segment LED or a single LED to be updated. Updating any front panel display parameter is accomplished in a similar manner for each parameter change. The display update requires the enable and the address line data to identify the parameter being changed.

3.3.8 TYPE 796375-1 DIGITAL MOTHERBOARD (A9)

The reference designation for this assembly is A9. Refer to **Figure 6-8** for the Type 796375-1 Digital Motherboard schematic diagram.

The two 16 key encoders (U1 and U2) contained on the motherboard receive input information from the Keyboard assembly (A13) and output valid data to the Interface subassembly (A9A3). Three digital subassemblies Microprocessor (A9A1), IEEE-488 Interface (A9A2) and Interface (A9A3) plug into the Digital Motherboard.

The Keyboard is divided into two matrices of four rows (X) and four columns (Y). With no key on the Keyboard depressed, the row inputs (the Xs) are pulled HIGH and the column outputs sequentially output a logic LOW. For example, depressing the keypad pushbutton, S13 for the Supergroup section causes no change while the X4 input is off, keeping the level HIGH at Y1. When the X4 column is scanned by encoder U1, the normally HIGH X4 goes LOW and Y1 goes LOW. This condition disables A1U9's internal counter resulting in the X4 line being kept LOW. When Y1 also goes LOW the key bounce circuit timing (controlled by C38 for U2 and by C34 for U1) is initiated and all other Y inputs are locked out. The combination of the halted counter value, the X value, and the decoded Y input. When the key bounce circuit times out, the input data is latched and the data available line (pin 12) goes HIGH signifying the presence of valid data at the output. Capacitor C36 is utilized to clock the internal counter of U1.

The Digital Motherboard distributes data from the Keyboard assembly (A13) through the Interface subassembly (A9A3) to the Display assembly (A1), to the Demodulator assemblies (A3-A8) and to any of the other assemblies or subassemblies affected by the changed data. The Digital Motherboard is the intermediary through which all parameter changes are directed. Routing of the data and signals are accomplished via the printed circuit tracks and the interconnecting wiring.

3.3.8.1 Type 796371-1 Microprocessor (A9A1)

The reference designation for this subassembly is A9A1. Refer to **Figure 6-9** for the Type 796371-1 Microprocessor schematic diagram.

The Microprocessor subassembly (A9A1) contains the microprocessor integrated circuit (U1) the Programmable Read Only Memory (PROM) integrated circuits (U4-U7), the Random Access Memory (RAM) integrated circuit (U8) and various other semiconductor devices. Microprocessor U1 provides the control for the internal operations and timing for the WJ-9518BE-9S. The microprocessor reads operating instructions from the PROMs and both stores (writes) and retrieves (reads) data from the RAM.

U1 is an 8-bit microprocessor that functions as the Central Processor Unit (CPU) for the WJ-9518BE-9S. Data to and from the microprocessor is transmitted over a 16-bit multiplexed bus. This multiplexed bus is divided into two separate buses. One-half of the bus is the high-order, 8-bit address bus. This portion of the bus carries address bits 8-15. The other

half of the bus carries the low-order 8-bits of the multiplexed address/data bus. This portion of the bus carries the 0-7 address bits and the 0-7 data bits.

Internal timing of the microprocessor clock frequency is provided via Y1 and its biasing network (R1, C1 and C2). Y1 is a crystal oscillator with a resonant frequency of 6.1444 MHz. Connecting the crystal oscillator to the X_{IN} (pin 11) and the X_{OUT} (pin 10) provides the microprocessor with an oscillator input frequency that is divided by 2 producing the 3.0722 MHz microprocessor clock frequency (pin 9). This clock frequency is utilized throughout the unit for timing, synchronization of events, exchange of data and address information.

Output address lines, A8-A12 from microprocessor U1 are applied to the address inputs of the 8K byte Programmable Read Only Memory (PROM) and the 2K byte Random Access Memory (RAM) integrated circuit. Multiplexed address/data lines (AD0-AD7) are applied to resistor network U17, 8-bit latch U2 and through U3 to the data lines of the PROMs and RAM. These address and data lines are applied to the IEEE-488 Interface and to the Interface subassemblies.

When the Address Latch Enable (ALE) (pin 30) changes from a HIGH level to a LOW level, the microprocessor indicates the presence of a valid Input/Output, Memory, (IO/ $\overline{M}$), or refresh address on the AD0-AD7 lines.

Selection of the PROMs (U4-U6) is accomplished via the 3-to-8 line address decoder U12. When the output from pin 31 (IO/ $\overline{M}$) of U1 is LOW, the three address outputs (AD13-AD15) enable the PROMs or RAM to be written into or read from. (Refer to **Table 3-3** for the address input to enable the various outputs.) Output enables for the RAM are applied to one input of the quad 2-input OR gate (U13). The other input to the OR gate is supplied from U14 of the power up/down circuit. As long as +5 Vdc is applied to the microprocessor the output of U14 is LOW. When both inputs to one of the OR gates are LOW, the resulting LOW output enables RAM U8 and allows access to the addressed memory location to retrieve (read) data. The power up/down circuit, composed of transistors Q1-Q3, U14, VR1, BT1 and their associated components, provides battery back-up for the unit operating parameters stored in RAM location when power to the unit is interrupted. This allows the unit to be turned off and turned back on without having to enter all of the operating parameters again. Removing power from the unit (power down) causes the +5 V supply to the Microprocessor subassembly (A9A1) to decrease. When the supply voltage decreases below 3.3 Vac, CR2 is forward biased by battery BT1. The output from BT1 is applied through R9 to U13, U14 and RAM U8.

When power is removed from the unit, the collector of transistor Q1 goes LOW. This LOW cuts off Q3, Q2 and causes BT1 to forward bias CR2. The LOW at the collector of Q1 is also applied to pin 1 of NAND gate U14A. A HIGH output from U14A pin 3 through the forward biased diode (CR1) to the inputs of NAND gate U14B. The resulting LOW at the output of U14B is applied to the inputs of NAND gate U14C and also to $\overline{NMI}$ Non-maskable Interrupt (pin 21) of the microprocessor (U1). $\overline{NMI}$ is held LOW for 22 m seconds by the RC time constant of R4 and C7. When the $\overline{NMI}$ line goes LOW, the microprocessor stores the data in its registers into RAM U8.

Table 3-3. Address Selection for the Chip Enable

Address Selected			Output								IC Enabled (Type)
A15	A14	A13	0	1	2	3	4	5	6	7	
0	0	0	0	1	1	1	1	1	1	1	U4 (PROM)
0	0	1	1	0	1	1	1	1	1	1	U5 (PROM)
0	1	0	1	1	0	1	1	1	1	1	U6 (PROM)
1	0	0	1	1	1	1	0	1	1	1	U8 (RAM)

The LOW input at U14C, from U14B, produces a HIGH at the output (pin 10) which is applied to one input of OR gates U13A, B, C and D and to both inputs of NAND gate U14D. U14D produces a LOW output to the $\overline{\text{RST IN}}$ (Reset Input) line of the microprocessor. This LOW at the $\overline{\text{RST IN}}$ causes the microprocessor to clear the internal registers, disables interrupts and generates a restart output pulse.

At power up, the +5 Vdc supply line voltage increases to its regulated voltage level. As the supply voltage rises above the threshold level determined by resistor R5 and zener diode VR1 (approximately 4.7 Vdc), Q1 is forward biased and conducts. When Q1 conducts, a HIGH is applied through R8 to the base of transistor Q2, through R7 to the base of Q3 and also to input pin 1 of NAND gate U14A. HIGHs at both inputs of U14A, produce a LOW output through CR1 to the inputs of NAND gate U14B. U14B produces a HIGH output to the microprocessor and to the inputs of U14C. A HIGH at the input of U14C is delayed 33 μsec by the RC time constant created by R2 and C6. When the input of U14C goes HIGH, the LOW at its output is applied to U13A through D and to U14D. A LOW at the inputs of U14D produces a HIGH at the output. This HIGH is applied to the $\overline{\text{RST IN}}$ (pin 33) of the microprocessor, allowing the microprocessor to restart its operations.

When transistor Q3 conducts, the output reverse biases CR2. With CR2 reverse biased, the battery backup voltage is replaced by the regulated supply voltage.

U15, U16 and U17 are resistor networks utilized as current limiting resistors for the multiplexed address/data lines (U17) and for the peripheral bus lines (U15 and U16). The peripheral bus lines (pins 7-20) allow control information to be exchanged between the microprocessor and the other functions the unit is performing.

3.3.8.2 Type 796373-1 IEEE Interface (A9A2)

The reference designation for this subassembly is A9A2. Refer to **Figure 6-10** for the Type 796373-1 IEEE Interface schematic diagram.

The IEEE Interface subassembly provides for remote communication operation via an external controller connected to the rear panel IEEE-488 connector (J1). This connector links the remote controller with the IEEE Interface subassembly providing for two-way communication between the controller and the demodulator. Data is transmitted over the DI01-DI08 lines. The remaining lines consist of the five interface management lines (ATN, SRQ, REN, EOI and IFC) and the three transfer control lines (DAV, NRFD and NDAC).

Together these lines form the IEEE-488/GPIB (General Purpose Interface Bus). The GPIB is a parallel interface bus with an asynchronous transfer of data, allowing for up to 15 devices to be connected together on the same bus. Protocol for the IEEE-488 GPIB requires that there be one system controller (a device to control the interface functions of the various devices on the bus), one talker (a device that transmits data) and the remaining devices on the bus as listeners (devices that receive data).

The GPIB consists of the eight data lines utilized to transfer data and commands between devices on the bus in conjunction with the help of the management and control lines. Each of the five management lines has a unique purpose. Attention line (ATN) is utilized to indicate that the controller has access of the bus and that the data on the lines is to be interpreted as a command. Service Request (SRQ) is utilized by a device to request service from the controller. Remote Enable (REN) is utilized by the controller to signify the source (remote or local) of the controller commands. End or Identify (EOI) is utilized either by a controller, along with ATN to demand a parallel poll, or by a talker to indicate the last byte of a data block. Interface Clear (IFC) causes the entire GPIB to enter into an idle state. Only the system controller is allowed to generate the IFC.

The three transfer control lines are utilized to conduct the asynchronous, interlocking, three-wire handshake. Data Valid (DAV) is initiated by a talker device to indicate the presence of valid data on the bus. Not Ready for Data (NRFD) is initiated by the listener devices to indicate that a listener is not ready to accept more data. Not Data Accepted (NDAC) is initiated by a listener device to indicate that all of the listeners haven't read the data lines yet.

Control of the IEEE-488 bus is accomplished via the asynchronous 3-wire handshake. Following is a description of the 3-wire handshake. Assume that a talker device on the bus is ready to transfer data. At the beginning of the handshake procedure, the NRFD (Not Ready for Data) line is LOW (false). This indicates that the listeners on the bus are ready to accept data. The NDAC (Not Data Accepted) line is HIGH (true), indicating that the listeners have not accepted the data. This is understandable, since no data has been set yet. The talker now places data on the data lines, waits for the required settling time, and then drives the DAV (Data Valid) line HIGH (true), indicating that the data is valid. Each active listener device on the bus drives their NRFD (Not Ready for Data) lines HIGH (true), to indicate that they are not ready to accept more data. Now these listener devices read the data and drive the NDAC line LOW (false), indicating acceptance. This causes the talker device to drive the DAV line LOW (false) and prepare for the transfer to the next data byte. Listener devices, responding to the LOW DAV, drive the NDAC line HIGH (true). Now the talker device can output a new data byte on the data lines and wait for the NRFD line to go LOW to start the next handshake cycle.

Data and signals present on the GPIB at the IEEE-488 connector (J1) is applied directly to transceivers U1 and U2. These transceivers are utilized to provide the current required to drive the interface bus. U1 receives and transmits data on the DIO lines. U2 passes the interface management and transfer control lines. When the transmit enable line (TE) at pin 1 of U1 and U2 is LOW, signals at J1 are input to U3. When the transmit enable line is HIGH, signals from U3 are output to J1.

U3 is a GPIB talker/listener that interfaces between the microprocessor (U1) of the Microprocessor subassembly and the IEEE Standard 488 digital interface bus.

Address switch S1 is utilized to set the unit 488 address. Options switch S2 is utilized to change the unit's 488 address via the front panel and to indicate the installed

options. When the switch contact is closed, a +5 Vdc is applied across the associated resistor network (U6 or U7) to transparent latches U4 and U5. Digital data from switches S1 and S2 are applied to the data inputs (D0-D7) of these latches. This input data is transferred to the output pins (Q0-Q7) whenever the latch enable (pin 11) is HIGH and the output enable (pin 1) is LOW. In this state, data at the latch input is coupled to the output and applied to the data bus port lines (D0-D7) of U3. Data cannot be written into or read from the internal GPIB registers unless U3's chip select ($\overline{CS}$) is LOW. The chip select line logic level is controlled by the microprocessor (A9A1-U2) read ($\overline{RD}$) and write ($\overline{WR}$) lines, pins 9 and 10 respectively, determining whether data is read from or written into the selected register. Register selection is controlled via the three register select lines (pins 21-23). **Table 3-4** illustrates the register select control.

Table 3-4. 8291A Register Select

Read Register	Register Select			Write Register
	RS2	RS1	RS0	
Data In	0	0	0	Data Out
Interrupt Status 1	0	0	1	Interrupt Enable 1
Interrupt Status 2	0	1	0	Interrupt Enable 2
Serial Poll Status	0	1	1	Serial Poll Mode
Address Status	1	0	0	Address Mode
Command Pass Through	1	0	1	Aux. Mode
Address 0	1	1	0	Address 0/1
Address 1	1	1	1	EOS

3.3.8.3 Type 796372-1 Interface (A9A2)

The reference designation for this subassembly is A9A3. Refer to **Figure 6-11** for the Type 796372-1 Interface schematic diagram.

Interface subassembly A9A3 transfers data between the Microprocessor (A9A1) and the Keyboard (A13), Display (A1) and Demodulator assemblies (A3-A8). Data to and from these assemblies is transmitted via the data bus lines (D0-D7). The microprocessor selects the address of the device via the A0-A7 address lines, and either a read or write enable to read ($\overline{RD}$) or write ($\overline{WR}$) to the devices on the Interface subassembly. Enabling the read or write line allows decoder/demultiplexer U6 to either read data from or write data into the selected device. **Table 3-5** illustrates the input logic level required to enable the various outputs. A LOW on the output line from U6 enables the device addressed on the output line.

Only when the $IO/\overline{M}$ line (P1 pin 19) is HIGH is data transferred through the Interface subassembly. A LOW at P1 pin 19 causes the output of U12A and U6 to go HIGH inhibiting their operation.

The 3.072 MHz clock pulse (P1 pin 7) from the microprocessor is applied to the clock input (pin 10) of binary ripple counter U15. U15 provides a 96 kHz output frequency at pin 3 which is applied to the clock input (pin 10) of binary ripple counter U17. Each of U17's successive outputs is one-half the frequency of the previous Q output stage. Output frequencies from U17 are applied to U18 and U19, and to several other devices on the Interface subassembly.

Table 3-5. Decoder/Demultiplexer Truth Table

Inputs						Outputs							
Enable			Select										
G1	G2A	G2B	A	B	C	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	H	L	L	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

With pin 15 grounded multiplexers U18 and U19, via the select line (pin 1), enable either the A or B input signal to be applied to the associated Y output. With the select line, HIGH, the B input signals are applied to the Y outputs and when the select line is LOW, the A input signals are applied to the Y outputs. Output signals from multiplexers U18 and U19 are applied to random access memory (RAM) U20. RAM U20 provides temporary storage for front panel digital display data.

Output Yc, from U19 is applied to both U20 and to pin 1 of octal transceiver U21. The direction of data flow through transceiver U21, is determined via the logic level at pin 1. A LOW at pin 1 allows data to flow from B to A and a HIGH allows data to flow from A to B. The direction of data flow through U21 is controlled by the logic level of the read line. A LOW on the read line ($\overline{RD}$) causes the data flow through U21 to be from B to A and allows the microprocessor to read the display data. Applying a LOW on the write line ($\overline{WR}$) allows U20 to write data to the digital displays.

During the time the microprocessor is reading data from or writing data to the digital display RAM, ripple counter U15 is reset via the HIGH applied to pin 11 from hex inverter U13D. Resetting U15 causes the output at pin 3 to go LOW and momentarily halt the counting of both U15 and U17. Halting the counting sequence allows time for the display data to be read from or written into RAM U20. Once the data has been processed, U15's reset line goes LOW and both U15 and U17 resume their counting.

Logic levels at the address (A0-A7), read ($\overline{RD}$) and write ($\overline{WR}$) lines are applied to the input gates of triple input NAND gates of U12. Outputs from U12 and address lines A4 and A5 are applied to the inputs of decoder/demultiplexer U6 to select the device. This selection is accomplished via the address and either a read or write pulse. Since the same address is used for two device circuits, the read and write lines determine which device is addressed. Refer to **Table 3-6** to determine which device is selected. Applying a LOW to the selected device enables its circuitry to operate. A LOW at U6 pin 15 is applied to the B input of multivibrator U5A. The negative output pulse from U5A is applied to pin 9 of OR gate U11C which causes the output of operational amplifier U10 to generate an output resulting in audible tone to be generated by LS1. This tone is generated for the duration of the RC time constant established by R1 and C3.

Table 3-6. Device Selection

Address								Device Selected	
MSB							LSB	Read	Write
1	1	0	0	1	1	1	1	U1, U2	(U5, U10, U11, LS1)
1	1	0	1	1	1	1	1	U9, U8	U3
1	1	1	0	1	1	1	1	U14	U4

The tone circuit, composed of U5A, U11C, U10, its biasing circuitry and LS1, is selected by a LOW from U6 pin 15 applied to U5A pin 2, producing a LOW output pulse at pin 4. This LOW pulse is directed to pin 9 of OR gate U11C. The other input to OR gate U11C is from pin 5 of binary counter U17. The output from U11C is applied through R8 to the inverting input (pin 6) of operational amplifier U10. Resistors R6 and R7 set up the bias voltage at pin 5. When the tone circuit is addressed, the LOW output from U11C causes a positive output from U10 to generate an audible tone via LS1. The tone is generated when an erroneous front panel parameter is entered.

Pressing a key on the Keyboard, outputs data from the 16-key encoders (A9U1 and A9U2) to U1, U2, and U11D of the Interface. Keyboard data is applied to U2 via the K0-K3 lines. Pressing keys S1 through S15 produce a HIGH at P2 pin 48, while pressing keys S16 through S30 produce a HIGH at P2 pin 46. These levels are sent to OR gate U11D and also to the set and reset inputs of dual D-type flip-flop U1. The output from OR gate U11D drives U1's clock input, causing the $\overline{Q}$ output to go LOW and sets the $\overline{INTR}$ line LOW. A HIGH at pin 48 produces a HIGH at the Q output (pin 13) of U1. When a HIGH at pin 46 is sent to U1, its Q output is LOW. The Q output from U1 is routed directly out P2 pin 44 to key encoder A9U1, through inverter U13B to A9U2 and also to the D4 data input of 8-bit latch U2. Only one output enable line, pin 44 or pin 49, is LOW at any one time when a keypad key is pressed. A HIGH at pin 48 results in a LOW at pin 44. A HIGH at pin 46 produces a LOW at pin 49.

Data applied to the D inputs of 8-bit latch U2 is applied to the Q outputs when the latch enable (pin 11) is LOW. When both the latch enable and the output enable (pin 1) are LOW, U2 is latched. This allows data at the D inputs to appear at the Q outputs without being inverted. Data at the Q outputs of U2 are applied to the data bus.

Reading the keyboard status is accomplished by using the same address code as for the tone circuit, except for a LOW on the read line instead of a LOW the write line. With the read line LOW, the output at U6 pin 4 is LOW. This LOW is applied to both U2 and U13C. LOWs at U2 pin 1 and pin 11 allow keyboard data applied to the D inputs to be present at the Q outputs. Data at U2's Q outputs are applied to the data bus lines D0-D7 and is read by the microprocessor. The LOW used to read the keyboard data is also applied through inverter U13C to reset the output of U1 (pin 2) HIGH.

The same LOW applied at U2 is also applied to pin 5 of hex buffer inverter U13C. U13C converts the input LOW to a HIGH at output pin 6 which is coupled directly to dual D-type flip-flop U1. This HIGH allows the $\overline{Q}$ and Q outputs to go HIGH and LOW, respectively. When the LOW at U3 pin 11 goes HIGH, data at the D inputs is applied to the noninverting Q

outputs. Outputs from octal D-type flip-flop U3 are applied to P2 pins 29-32 and pin 34 and also to pins 9-11 of U7. Data applied to P2 pins 29-31 and pin 34 are directed to the selected demodulator via software control. Data coupled from U3 to multiplexer U7 determines which one of the six input lines is selected. These input lines are from the front panel GAIN level controls in the form of an analog voltage. Via the data applied to the input control lines (pins 9-11), U7 determines which gain level voltage is sent out pin 4 to the analog-to-digital converter U8.

Using the same address required to select U3 and applying a LOW to the read line, instead of the write line, applies a LOW from U6 to both U8 and U9. U8 is an analog-to-digital converter and U9 is a latch. Analog voltages from multiplexer U7 are applied to pins 3 and 4 of the analog-to-digital converter (ADC). Analog-to-digital converter (ADC) U8 uses the successive approximation technique to convert the analog voltage at pin 4 to a digital approximation of the input voltage. This digital approximation data is placed on the data output pins (DB0-DB7). The reference voltage utilized by ADC U8 is derived from the regulated +5 V applied through the voltage divider network of R2 and R3 to the inverting input of operational amplifier U10. The output voltage from U10 is at a -5 Vdc level.

With the chip select line held LOW, U8 operates in the read only memory (ROM) interface mode. In the ROM mode converter operation is controlled by the read input. Applying a LOW at the read input (pin 15) causes U8 to initiate a data read. A data read can only be accomplished when the busy line (pin 14) is HIGH. If the busy line is LOW and a read is attempted, erroneous data will be read. The busy line is set HIGH when the ADC conversion process is complete. The rate of conversion is determined by the RC time constant of R5 and C7. When the conversion process is completed and the busy line is HIGH, a LOW on the read line causes U8 to output digital data to latch U9. With U9's latch enable tied HIGH, data applied to the D inputs is transferred to the Q outputs and onto the data bus.

Enabling dual D-type flip-flop U14, via the address and read data applied to U6, the LOW from U6 causes U14 pin 8 output to be returned HIGH. Pin 8 is set LOW by the clock pulse from timer U17. This LOW is sent to the microprocessor and is used in determining the length of the dwell time. A LOW at U14 pin 13 resets U14, returning the RSTC line HIGH.

A LOW from U6 applied to pin 11 of octal D-type flip-flop U4. During the LOW-to-HIGH transition of the clock pulse, at pin 11, data at the D inputs is coupled to the Q outputs. These Q outputs determine which demodulator is enabled via applying a HIGH to the selected demodulator's enable line (ENB0-ENB6).

Twelve stage binary counter U17 receives a 96 kHz clock pulse at pin 10 from counter U15. U17 utilizes this 96 kHz clock frequency to produce lower frequencies used to clock various devices on the interface board. Frequency outputs from U17 are applied to U18, U19, U11A, U16, U11C, U14 and the display address lines DA0-DA3. Applying a HIGH to U17 pin 11 from the display board counter, via P2 pin 8, resets all of U17's Q outputs to 0.

When U17 is counting several of its output frequencies are applied to decoder/demultiplexer U16. **Table 3-5** illustrates the input levels required to select the possible outputs. LOW outputs from U16 are applied to the digital display as display strobes (DST0-DST3). Display strobes from U16 are output on odd clock pulses. Display strobes from U16 are inhibited by OR gate U11A for a period of 63 clock pulses. The LOW output from pin 11 of U16 is applied to the negative trigger input of multivibrator U5B. With pin 9 of 5B LOW, the $\bar{Q}$ output (pin 12) produces a LOW pulse. The duration of the output pulse from U5B

is determined by the RC time constant established by R10, R11 and C11. This RC time is variable from approximately 22 μ seconds to 522 μ seconds. Varying the RC time constant via R10 varies the brightness of the front panel display.

When the level at pin 8 of P2 is HIGH, counter U17 is reset. This HIGH at P2 pin 8 is inverted through U13F applying a LOW to multivibrator U5B causing it to reset.

3.3.9 TYPE 766013-1 POWER SUPPLY REGULATOR (A14)

The reference designation for this assembly is A14. Refer to **Figure 6-16** for the Type 766013-1 Power Supply Regulator schematic diagram.

3.3.9.1 Part 380653-1 Power Supply Regulator No. 1 (A14A1)

The reference designation for this subassembly is A14A1. Refer to **Figure 6-16** for the Type 380653-1 Power Supply Regulator PC Assembly No. 1 schematic diagram.

Power Supply Regulator Assembly Number 1 produces the regulated +15 Vdc and -15 Vdc from the ac voltage. After being filtered through FL1 and coupled through transformer T1 the ac line voltage is applied to E1 and E3. The ac voltage at E1 is applied to full-wave rectifier CR1 and CR3 and the line voltage at E3 is applied to full-wave rectifier CR2 and CR4. On the positive half-cycle, diodes CR1 and CR2 are forward biased and conduct. On the negative half cycle, diodes CR3 and CR4 are forward biased and they conduct. This provides dual full-wave rectification for the transformer coupled ac voltage. Diodes CR1 and CR2 provide positive, full-wave rectification and CR3 and CR4 provide negative full-wave rectification. Capacitors C1 and C2 provide simple filtering for their respective full-wave circuit. Capacitor C1 increases the average positive dc voltage applied to E4 and C2 increases the average negative voltage applied to E7. These capacitors provide filtering by charging to the input peak ac voltage value, C1 charges positively and C2 charges negatively.

Capacitor C3 filters the ac component from the positive full-wave rectified voltage before being applied to E4 and the input of the positive 15 volt regulator (U1). Capacitor C4 filters the ac ripple from the negative full-wave rectified voltage before it is applied to E7 and the input of the negative 15 volt regulator (U2).

Two identical voltage divider networks control the output voltage from each regulator. Resistors R1, R2 and R3 form the voltage divider network for the +15 V adjustable regulator (U1). Resistors R4, R5 and R6 form the voltage divider network for the -15 V adjustable regulator (U2). Variable resistors R2 and R5 respectively control the regulated +15 Vdc and -15 Vdc outputs. Additional filtering of the positive regulator voltage is provided by C5 and C7 while C6 and C8 provide additional filtering for the negative voltage regulator.

These regulated +15 Vdc and -15 Vdc output voltages are utilized throughout the unit. Additional filtering of the supply voltages is provided on the assemblies and sub-assemblies.

3.3.9.2 Part 380668-2 Power Supply Regulator No. 2 (A14A2)

The reference designation for this subassembly is A14A2. Refer to **Figure 6-16** for the Type 380668-2 Power Supply Regulator PC Assembly No. 2 schematic diagram.

Power Supply Regulator Assembly Number 2 provides unregulated +8 Vdc for the front panel displays, the regulated +5 Vdc utilized throughout the unit and the regulated +27 Vdc applied to the LO synthesizer modules. Transformer coupled ac voltages are applied from E1 to E3 to full-wave diode rectifier U1. As the phase of the input ac voltage decreases from its peak positive value, capacitor C1 begins to discharge. The discharging of C1 provides a form of simple filtering by reducing the amount of ac ripple on the output of the rectified voltage. When the phase of the input voltage goes negative, the diode at pin 3 of U1 is forward biased and it conducts causing C1 to again charge to a peak positive value. As the phase of the input ac line voltage goes positive, capacitor C1 again begins to discharge causing an increase in the average dc voltage value and a decrease in the ripple on the rectified output. The full-wave rectified voltage receives additional filtering from C2 of any high frequency ac signal before being applied to the input of linear regulator U2. U2 is a positive voltage regulator with over-voltage protection.

Full-wave rectified input voltages are applied to pins 1 and 7 of regulator U2. This rectified input voltage is also applied through L1 to pin 6 of U2 and to E4. E4 is connected to the emitter of power transistor Q1. The output voltage from U2 pin 12 is applied directly to the base of power transistor Q1. The output voltage from the collector of Q1 is filtered by C5 and is fed through R7 to the inverting input (pin 9) of U2. Pin 9 is the inverting input to the internal overvoltage and undervoltage protection circuits. Pins 14 and 15 form the overvoltage and shutdown circuits. Whenever an overvoltage or undervoltage condition is detected at pin 9, that exceeds the fault delay time constant established by the value of C4, the overvoltage latch is set. Setting the overvoltage latch causes the level at pins 14 and 15 to be pulled LOW, disabling the driver output. With the fault condition corrected, pins 14 and 15 are reset, the driver output is enabled again and Q1 conducts again. The regulated +5 V from Q1 is further filtered by C6 and then split. One voltage path is to J1 as the +5 V output voltage and the other path is to the input (pins 1, 2 and 3) of dc-dc converter U3. In addition to the +5 V applied to U3, at pins 1, 2 and 3, +15 V from J1, pin 21, is also applied to U3 (pins 10 and 11). Grounding the negative voltage inputs (pins 22, 23 and 24) and applying +15 volts at the negative voltage outputs (pins 10 and 11) and produces a +27 Vdc output at pin 15. The +27 volt output from U3 is LC filtered by L1, C7 and C8 before being applied to J1 and to the LO synthesizer modules. Zener diode CR1 provides overvoltage protection for the dc-dc converter. Voltage in excess of 5.6 Vdc are shorted to ground through CR1.

When the unit is powered up, diode CR2 is forward biased, providing a current path for the +15 V supplying voltage, until the dc-dc converter's oscillator is stabilized. The output voltage from U3 reverse biases CR2 and the +15 V current path is to dc-dc converter U3.

SECTION IV
MAINTENANCE

SECTION IV

MAINTENANCE

4.1 GENERAL

The WJ-9518BE-9S FDM Demodulator has been designed to operate for extended periods of time with a minimum of routine maintenance. Cleaning, inspection and performance testing should be performed at regular intervals, consistent with the facility's normal scheduling, and after repairs have been completed.

4.2 CLEANING AND LUBRICATION

This unit should be kept free of dust, moisture, grease and other foreign matter to ensure trouble-free operation. Use low pressure air, if available, to remove accumulated dust from the interior of the demodulator. A clean, dry cloth or soft bristled brush may also be used for this purpose. No lubrication is required.

4.3 INSPECTION FOR DAMAGE OR WEAR

Many existing or potential troubles can be detected by making a thorough visual inspection of the unit. For this reason one of the first maintenance steps for an inoperative unit should be a complete visual inspection. Mechanical parts, such as pin connectors and interconnecting cables, should be checked for looseness, wear and other signs of deterioration. Plug-in assemblies and subassemblies should be checked to make sure they are properly inserted into the correct connector slot and making good physical contact. Electronic components showing signs of deterioration such as overheating, should be inspected along with a thorough check of the associated circuitry to verify proper operation. Damage due to overheating is often the result of related, but less apparent, problems in the circuit.

4.4 TEST EQUIPMENT REQUIRED

The test equipment listed in **Table 4-1**, or its equivalent is required to perform the following troubleshooting procedures, performance testing and alignment procedures.

4.5 TROUBLESHOOTING PROCEDURES AND FAULT ISOLATION

Troubleshooting of the WJ-9518BE-9S FDM Demodulator can be performed by placing the unit in local control and observing its operation while varying the operating parameters. To eliminate the possibility of external conditions causing the malfunction, utilize an appropriate signal generator, listed in **Table 4-1**, to inject the required test signal while monitoring the output signals.

The Troubleshooting Table (**Table 4-2**) and performance tests listed in the following paragraphs are provided as an aid for localizing the cause of a malfunction to a particular

assembly or subassembly within the unit. References should also be made to the block diagrams, provided in **Section III**, and the schematic diagrams, provided in **Section VI**, to aid in fault isolation.

Table 4-1. Test Equipment Required

Equipment	Type	Manufacturer
Autotransformer	W5MT3W	General Radio
ACVM (2)	3400A RMS	Hewlett-Packard
RFVM	92B	Boonton
"T" Adapter	91-14A	Boonton
50 Ω Termination	91-15A	Boonton
Hi Z Probe	91-12F	Boonton
Oscilloscope	T935A	Tektronix
Digital Voltmeter	8050A	Fluke
Function Generator	HP 3325A	Hewlett-Packard
Remote Controller	HP 8525S	Hewlett-Packard
50-75 Ohm Adapter	-	Various
75 Ohm Load (2)	-	Various
600 Ohm Load (2)	-	Various
Spectrum Analyzer	HP 3585A	Hewlett-Packard
Frequency Counter	HP 5315B	Hewlett-Packard

NOTE

To prevent damage to the demodulator circuitry, de-energize the unit before removing or installing any assembly or subassembly.

Table 4-2. WJ-9518BE-9S Troubleshooting Table

Symptom	Probable Cause	Corrective Action
No Front Panel Display	Not Turned On	Move power switch to ON position.
	Switch S1 In Wrong Position	Ensure S1 is in the proper position for the applied line voltage.
	Blown Fuse	Correct cause of blown fuse and replace the blown fuse.
	Defective +8 V	Check the Power Supply voltages (para. 4.6.1).
No Baseband Output at A11J7	No Baseband Input A11J6	Verify the presence of a useable baseband signal at A11J6.

Table 4-2. WJ-9518BE-9S Troubleshooting Table (Cont'd)

Symptom	Probable Cause	Corrective Action
All LOs Unlocked	Reference Generator Module (A12) Defective	Verify the presence of a 1 MHz signal at A12J2-A12J8.
	Reference Selection Switch in Wrong Position	Ensure proper S3 reference switch position (INT/EXT) Verify proper Reference Generator performance (para. 4.6.3).
No Audio Output from any Demodulator	Baseband Amplifier (A11) Defective	Verify the Baseband Amplifier operation (para. 4.6.2).
	JW1 of the Input Converter (AXA1) Removed	Ensure the jumper wire (JW1) is installed (para. 4.7.5).
	Frequency Converter (AXA2) Faulty	Verify proper operation of the Frequency Converter (para. 4.6.8).
	Defective Digital Motherboard (A9)	Verify operation of the digital circuits (para. 4.6.4).
No Fine Tuning	Faulty Keyboard (A13)	Verify proper Keyboard operation (para. 4.6.4).
	3rd LO (A10) Defective	Ensure 3rd LO operation (para. 4.6.5).
No Headphone Output	Defective Headphone Amp (A2)	Verify Headphone Amplifier operation (para. 4.6.8).
Low Headphone Output	Gain Controls Misadjusted	Check GAIN/LEVEL controls

4.6

PERFORMANCE TESTING

The following test procedures may be used as a guide for periodic performance testing, as an aid in troubleshooting or as a functional check after repairs have been completed. Performance tests should be performed only by qualified technicians, using the test equipment listed in **Table 4-1** or their equivalent.

Unless otherwise specified, each of the demodulators should be set to the standard test settings listed in **Table 4-3** for each of the performance tests.

Table 4-3. Demodulator Standard Test Setting

Parameter	Setting
Demod Select	As Required
Tuned Freq	1000 kHz
PHONE Level	Mid Range
GAIN Level	Nominal
CONTROL	Local
Mode	Upright
FINE TUNE	0 Hz
SCAN DWELL	2 SEC
F kHz	2 kHz
F1	1 kHz
F2	15 MHz
BRIDGING	1-6
REF SEL	INT

4.6.1 POWER SUPPLY PERFORMANCE TESTS

1. Before applying power to the unit, ensure rear panel switch S1 is set to either the 110 Vac or the 220 Vac position depending on the line voltage utilized.
2. Connect the unit power cord to the variable autotransformer.
3. Set the autotransformer output voltage to minimum and turn on the autotransformer and the WJ-9518BE-9S Demodulator.
4. Increase the autotransformer output voltage while observing the autotransformer ampere meter. At line voltage level, the meter should not indicate above 0.5 amperes at 115 Vac.
5. Measure the power supply voltages at the test points listed in **Table 4-4**.
6. Using a times 1 (1x) probe, connect the AC coupled oscilloscope to each test point. Vary the line voltage +10% and -10% while monitoring the oscilloscope. Verify that the AC ripple is not greater than 50 mV peak-to-peak.

Table 4-4. Power Supply Voltages

Test Point		Voltage	Tolerance
A14A1	TP1	+15 Vdc	±0.05 V
	TP2	-15 Vdc	±0.05 V
A14A2	TP1	+8 Vdc	±0.03 V
	TP2	+5 Vdc	+0.2 V, -0.0 V
	TP3	+27 Vdc	21 V min

4.6.2 BASEBAND AMPLIFIER PERFORMANCE TEST

1. Connect the test equipment as illustrated by the dotted line and set a reference level on ACVM(B) of -10 dBm by varying the signal generator output level in **Figure 4-1**.

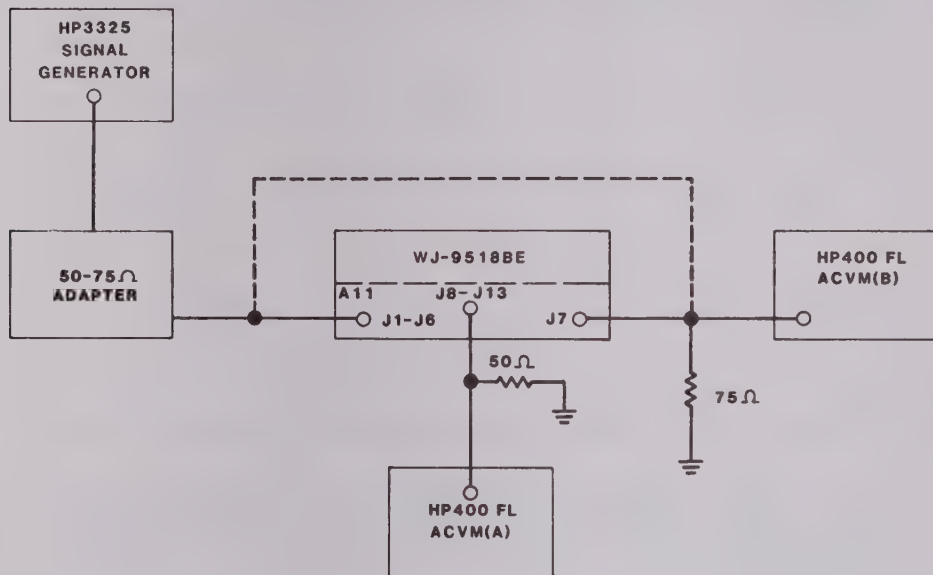


Figure 4-1. Baseband Amp Performance Test, Equipment Connection

2. Connect the test equipment as illustrated by the solid lines in **Figure 4-1** and tune the signal generator to 1001 kHz.
3. Measure the output level at A11J7. It should be -10 dBm (± 0.5 dB) at the baseband outputs A11J8-A11J13.
4. Measure the baseband output level at A11J7. It should indicate -10 dBm (± 0.5 dB) on the ACVM.
5. Remove all input bridging (press the INP BRG key and then the 0 numeral key) and observe the output level at ACVM(B). The level should drop more than 50 dB. The output level at A11J8 should still indicate -16.5 dBm (± 0.5 dB).
6. Select DEMOD 2 through DEMOD 6 and measure the output level for each associated demodulator (J9-J11). The output level should be -16.5 dBm (± 0.5 dB).
7. Reconnect the Baseband Amplifier outputs to Demodulators A3-A8.

4.6.3

REFERENCE GENERATOR PERFORMANCE TESTS

1. With rear panel switch S3 in the internal (INT) position, connect the test equipment as illustrated in **Figure 4-2**. Note: The unit should be on at least 30 minutes to allow the TCXO frequency to stabilize. Measure the frequency and output level at J2 through J8. The output should be 1 MHz (± 3 Hz) at 1.5 Vrms (± 200 mV).

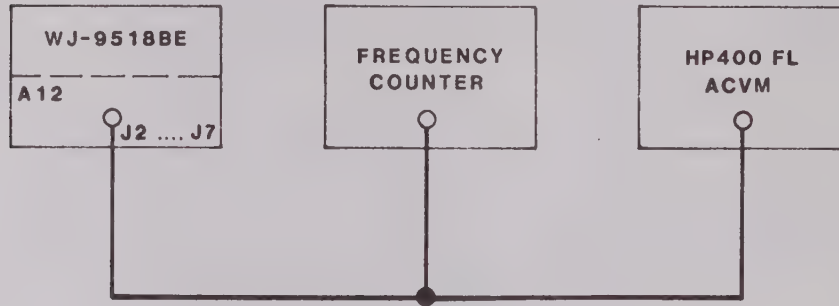


Figure 4-2. Reference Generator Performance Test, Equipment Connections

2. Move switch S3 to the external (EXT) position and observe the output level at the Reference Generator outputs. The output level should drop a minimum of 30 dB. Return the ACVM to the same range as in step 1.
3. Connect the test equipment as illustrated in **Figure 4-3**.

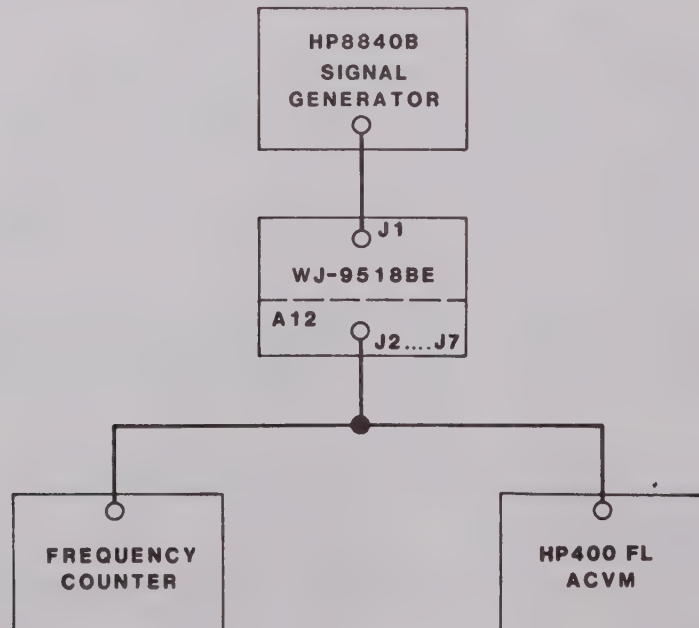


Figure 4-3. Reference Generator External Performance Test, Equipment Connections

4. Set the signal generator to 1 MHz CW at 0 dBm.
5. Measure the Reference Generator output frequency and output levels. The outputs should indicate 1 MHz (± 1 Hz) at 1.5 Vrms (± 200 mV).
6. Reconnect the Reference Generator outputs to the Demodulators (A3-A8) and the 3rd LO Synthesizer (A10).
7. Disconnect the test equipment.

4.6.4

KEYBOARD AND DISPLAY PERFORMANCE TESTS

1. Select local control for the WJ-9518BE-9S.
2. Select DEMOD 1 and verify the SEL single LED illuminates. (Display intensity may be varied via A9A3R10).
3. Press the UPR/INV key several times and verify the U and I single LEDs alternately and extinguish.
4. Depress the 960/2700 key several times and ensure the two LEDs for the CCITT PLAN illuminate, one at a time, and then both extinguish signifying selection of direct tuning. After cycling through once, observe the selected DEMOD display. With the LED for the 2700 CH plan illuminated, the DEMOD display should indicate:

0.0.0.0.00.

With the LED for the 960 CH plan illuminated, the selected DEMOD display should indicate:

00.0.00.

With both LEDs for the CCITT PLAN extinguished, the selected DEMOD display should display the frequency to which the demodulator was last tuned.

5. Select direct tuning, enter 1 and press the ΔF kHz key (for a 1 kHz step size). Utilize the ($\uparrow$) increment key to tune the DEMOD frequency from 01000 to 01010 and verify the numerical sequence from 0 through 10.
6. Tune the DEMOD frequency from 01010 to 01000 via pressing the ($\downarrow$) decrement key and verify the numerical sequence from 10 to 0.
7. Repeat steps 5 and 6 with step sizes of 10 kHz, 100 kHz, 1 MHz and 10 MHz to verify proper LED operation and numerical sequencing.

8. Select the 2700 CCITT Plan and utilizing the SMG, MG, SG, GP and CH keys to enter a valid CCITT frequency. (Refer to **Table 2-3**, and **Table 2-4**, for the valid ranges of each CCITT Plan.) Depress the TUNE key to tune the demodulator frequency.
9. Press the CH key and then press the increment and decrement keys to vary the selected channel across its entire range, from 01 to 12 and back to 01.
10. Repeat step 9 for the group and supergroup for both the 2700 and 960 channel plans and for the mastergroup and supermastergroup (2700 channel plan only) to verify the CCITT tuning scheme.
11. Repeat steps 2 through 10 for each of the five remaining demodulators.
12. Press the INP BRG key and then press the 0 key. Verify that no front panel LED beneath INPUT BRIDGING is illuminated.
13. Press the INP BRG key and then numerical keys 1 and 2. Observe that the 1-2 LED is illuminated. Press numerical keys 2 and 3, 3 and 4, 4 and 5, 5 and 6. Verify the associated LED is illuminated for each pair of numbers.
14. Press the INP BRG key and then press the 0 key. Observe that no bridging LED is illuminated.
15. Press the 960/2700 key to select direct tuning (both CCITT Plan LEDs are extinguished).
16. Press the FINE TUNE key and the increment key. Observe the LED for FINE TUNE is illuminated and that FINE TUNE/SCAN DWELL display indicates 5.
17. Press the increment key repeatedly until the FINE TUNE/SCAN DWELL displays 50.
18. Press the decrement key until the display indicates -50.
19. Reset the fine tuning frequency to 0. (The FINE TUNE front panel LED is not extinguished until after pressing another function key.)
20. Press the SCAN DWL key and numerical keys 1 and 0. Observe that the FINE TUNE - SCAN DWELL display shows "d 1.0".
21. Use the increment and decrement keys to vary the dwell time between 9.9 and 0.2, after the SCAN DWL key has been pressed.
22. Set the unit to the parameters listed in **Table 4-3** and depress the SCAN STRT key. Verify that the DEMOD 1 displayed frequency is incrementing and the LED for SCAN ON is illuminated.

23. Press the SCAN STOP and verify the DEMOD 1 frequency is no longer scanning and the LED for SCAN ON is extinguished.
24. Press the SCAN STRT key again and verify that the frequency scan resumes and the LED for SCAN ON is illuminated again.
25. Repeat steps 22 through 24 for the other demodulators.

4.6.5

3RD LO PERFORMANCE TESTS

1. Connect the test equipment as illustrated in **Figure 4-4**.

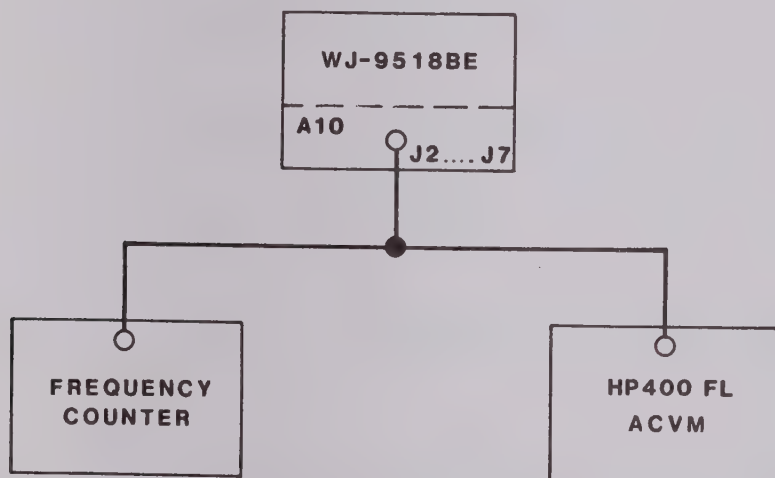


Figure 4-4. 3rd LO Performance Test, Equipment Connections

2. The outputs (J2 through J7) from A10 should be 500 kHz at a 120 mV (± 100 mV) level.
3. Set the FINE TUNE to +50 Hz and measure the 3rd LO frequency. It should read 500.050 kHz (± 1 Hz).
4. Set the FINE TUNE to -50 Hz and measure the 3rd LO frequency. It should indicate 499.950 kHz (± 1 Hz).
5. Reset the FINE TUNING to 0 Hz. The frequency counter displays 500 kHz and the FINE TUNE front panel LED is extinguished after pressing the TUNE key.
6. Remove the test equipment and reconnect the cables to their proper connectors.

4.6.6 2ND LO PERFORMANCE TESTS

1. Connect the test equipment as illustrated in **Figure 4-5**.

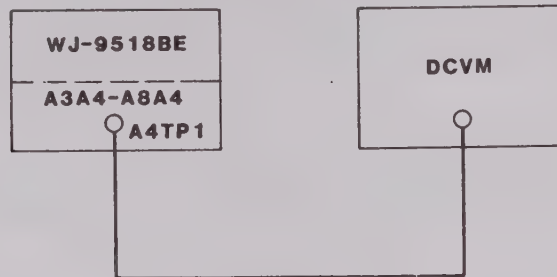


Figure 4-5. 2nd LO Performance Test, Equipment Connections

2. Set the unit to the Upright mode of operation and measure the tuning voltage. The tuning voltage should be 14.7 Vdc (+1 V, -2 V).
3. Observe the 2nd LO unlock LED (A4DS1) and verify that it is not illuminated.
4. Set the unit to the Inverted mode and measure the 2nd LO tuning voltage.
5. The tuning voltage should be 4.5 Vdc (+1 V, -2 V).
6. Repeat steps 2 through 5 for each demodulator's 2nd LO. If any of the 2nd LO unlock LEDs are illuminated, refer to the 2nd LO Alignment Procedure.
7. Disconnect the test equipment.

4.6.7 1ST LO PERFORMANCE TEST

1. Connect the test equipment as illustrated in **Figure 4-6**.

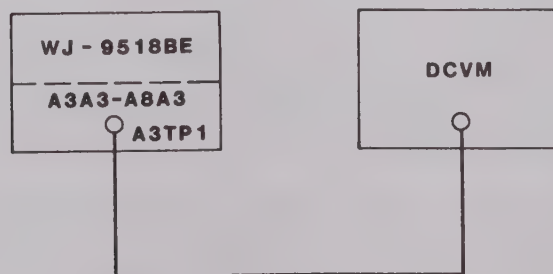


Figure 4-6. 1st LO Performance Test, Equipment Connections

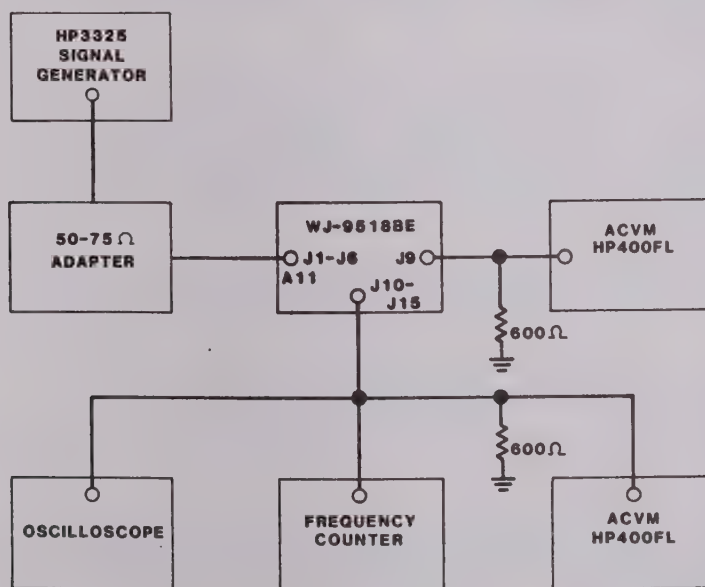
2. Tune the unit to 15000 kHz in the Upright mode and verify that the 1st LO unlock LED (A3DS1) is not illuminated. If the unlock light is illuminated, refer to the 1st LO Alignment Procedure.
3. Refer to **Table 4-5** for the 1st LO tuning voltage for the listed tuned frequencies in the Upright mode of operation.

Table 4-5. 1st LO Output Frequency

Tuned Frequency	1st LO Tuning Voltage
15000	15.5 Vdc (± 0.8 V)
11250	17.5 Vdc (± 0.8 V)
11251	5.6 Vdc (± 0.8 V)
7001	6.3 Vdc (± 0.8 V)
4001	5.6 Vdc (± 0.8 V)
000	4.6 Vdc (± 0.8 V)

4.6.8 DEMODULATOR PERFORMANCE TEST

1. Connect the test equipment as illustrated in **Figure 4-7**.

**Figure 4-7. Demodulator Performance Test, Equipment Connections**

2. Set the signal generator to 999 kHz, Sine with -32 dBm output level and the unit to 998 kHz, Upright mode. Set all GAIN controls to NOMINAL.
3. Observe the output indications on the test equipment and note the frequency. Verify the presence of an output signal at the PHONES connector (J9) of 2.45 Vdc (min.). Verify the presence of an output signal of 1.0 V (± 0.2 V) and a frequency of 1 kHz (± 1 Hz) at J10.
4. Press the FINE TUNE key and increase the fine tuning 50 Hz via the increment key. Verify the frequency observed at J10 is approximately 50 Hz (± 1 Hz) lower in frequency than noted in step 3.
5. Press the decrement key until the FINE TUNE display indicates a -50. Measure the frequency at J10 is 50 Hz higher in frequency than noted in step 3.
6. Reset the fine tuning to 0 Hz and observe that the displayed frequency on the frequency counter is the same as noted in step 3.
7. Depress the 1 key, and then press the ΔF kHz key. Observe the number displayed in the DEMOD 1 display is 1.
8. Press the decrement key and verify the output signal at J10 is 2 kHz and DEMOD 1 indicates 997 kHz. Press the decrement key again and verify a 3 kHz (± 1 Hz) output at J10. Verify DEMOD 1 displays 996 kHz.
9. Press the decrement key again and verify the output signal level on the ACVM, at J10, drops off 15 dB or more and DEMOD 1 displays 995 kHz. Press the decrement key again and verify the output level is 30 dB or more below the level noted in step 3 and DEMOD 1 displays 994 kHz.
10. Depress the UPR/INV key and verify the I (inverted) LED is illuminated. Reset the ACVM to the same range as in step 3.
11. Press the increment key twice and verify the presence of a 1 kHz signal at J10 and DEMOD 1 displays 996 kHz.
12. Press the decrement key again and verify the output at J10 is a 2 kHz signal (± 1 Hz).
13. Ensure that depressing the decrement key again produces a 3 kHz signal at J10 and DEMOD 1 displays 998 kHz. Note the output level on the ACVM.
14. Press the increment key two more times and observe the demodulator output level at J10 and verify the output level decreased at least 30 dB from the level noted in step 13.

- 15. Repeat steps 2 through 14 for the other five Demodulator assemblies.

Connect the equipment as follows for each Demodulator.

<u>Sig. Gen.</u> <u>To:</u>	<u>For</u> <u>Demodulator</u>	<u>ACVM</u> <u>To:</u>
A11J2	2	J11
A11J3	3	J12
A11J4	4	J13
A11J5	5	J14
A11J6	6	J15

4.7 ALIGNMENT PROCEDURES

The following alignment procedures should not be performed on a routine basis. These procedures should be followed after components have been replaced or to spot align a module after it has been replaced. Only after it has been determined that alignment is necessary, should any adjustment be made.

4.7.1 **POWER SUPPLY ALIGNMENT PROCEDURES**

- 1. Connect the test equipment as illustrated in **Figure 4-8** via the solid lines.

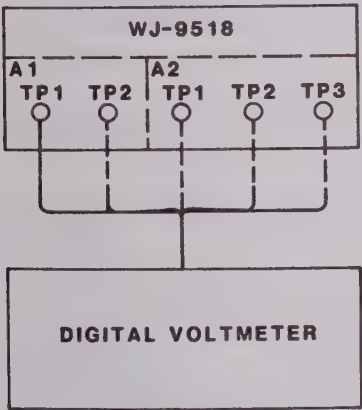


Figure 4-8. Power Supply Alignment, Equipment Connections

- 2. Measure the voltages at the test points listed below. Ensure the voltage measured is within the tolerance listed in **Table 4-6**.
- 3. Disconnect the test equipment leads.

Table 4-6. Power Supply Alignment Voltages

Test Point		Measurement	Tolerance	Adjustment
A1	TP1	+15 Vdc	± 0.05 V	R2
A1	TP2	-15 Vdc	± 0.05 V	R5
A2	TP1	+8 Vdc	± 0.03 V	
A2	TP2	+5 Vdc	-0 V, +0.2 V	
A2	TP3	+24 Vdc	21 V (min)	

4.7.2

1ST LO ALIGNMENT PROCEDURE

1. Connect the test equipment as illustrated by the solid lines in **Figure 4-9** and select DEMOD 1.

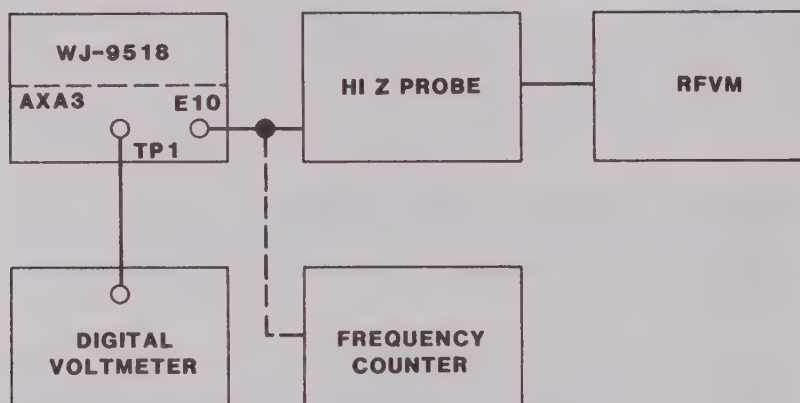


Figure 4-9. 1st LO Tuning Voltage Equipment Connections

2. Tune the selected Demodulator to 15000 kHz.
3. Observe the indicated voltage on the voltmeter and adjust C27 to produce a reading of 15.50 Vdc at AXA3 TP1.
4. Tune the Demodulator to 11250 kHz and adjust C52 to produce a voltage of 17.53 Vdc at AXA3 TP1.
5. Tune DEMOD 1 to the frequencies listed in **Table 4-7** and verify the output levels, frequencies, and tuning voltages correspond to the tuned frequency. Connect the RFVM and measure the output level and then disconnect the RFVM. Connect the frequency counter and measure the tuned frequencies.
6. Repeat steps 2 through 5 for Demodulators 2 through 6.
7. Connect the test equipment as illustrated in **Figure 4-10**.

Table 4-7. 1st LO Alignment

Tuned Frequency		Upr	Inv	RF Level
15.5 V (± 0.8 V)	15000 kHz	40 MHz	40.004 MHz	-5 dBm (± 1 dB)
17.536 V (± 0.8 V)	11250 kHz	36.250 MHz	36.254 MHz	-5 dBm (± 1 dB)
5.63 V (± 0.8 V)	11251 kHz	36.251 MHz	36.255 MHz	-5 dBm (± 1 dB)
6.15 V (± 0.8 V)	7001 kHz	32.001 MHz	32.005 MHz	-5 dBm (± 1 dB)
15.53 V (± 0.8 V)	7000 kHz	32.000 MHz	32.004 MHz	-5 dBm (± 1 dB)
5.65 V (± 0.8 V)	4001 kHz	29.001 MHz	29.005 MHz	-5 dBm (± 1 dB)
4.68 V (± 0.8 V)	0 kHz	25.0 MHz	25.004 MHz	-5 dBm (± 1 dB)

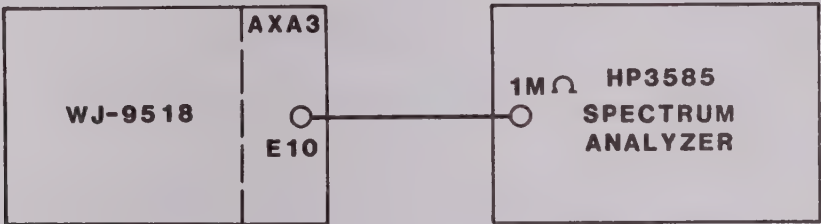


Figure 4-10. 1st LO Spur Adjustment Equipment Connections

- Set the spectrum analyzer controls to display a 500 Hz frequency span, with a start frequency of 25 MHz, a stop frequency of 25.0105 MHz and centered at 25.01 MHz.
- Tune DEMOD 1 to 0 kHz in the Upright mode and adjust R7 to reduce the level of the 8 kHz spur as far as possible.
- Repeat steps 7 through 9 for Demodulators 2 through 6.
- Disconnect all test equipment.

4.7.3 2ND LO ALIGNMENT PROCEDURE

- Connect the test equipment as illustrated in **Figure 4-11** by the solid lines and select DEMOD 1.
- With the digital voltmeter connected to AXA4 TP1, select the Upright (U) detection mode.
- Observe the tuning voltage displayed on the digital voltmeter. It should indicate 14.7 Vdc (+1 V, -2 V) typically. Verify the output level on the RFVM is -5 dBm (± 1 dB). Disconnect the RFVM and connect the frequency counter. Verify the output frequency is 25.5 MHz.

4. Select the Inverted (I) detection mode and observe that the voltmeter indicates 4.5 Vdc (+1 V, -2 V) typically. Verify the output frequency is 24.5 MHz. Disconnect the frequency counter and connect the RFVM. Verify the output level is -5 dBm (± 1 dB).
5. Repeat steps 2 through 4 for Demodulators 2 through 6.

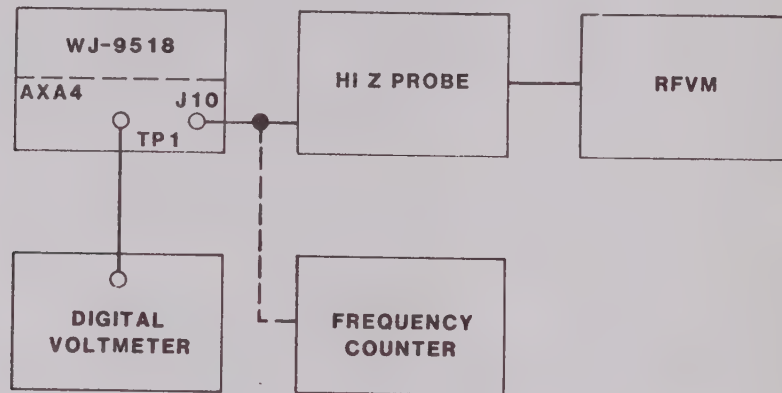


Figure 4-11. 2nd LO Alignment Procedures, Equipment Connections

4.7.4 3RD LO ALIGNMENT PROCEDURE

1. Connect the test equipment as illustrated by the solid lines in **Figure 4-12**. Note: Allow the 3rd LO a minimum of 2 minutes to stabilize before alignment.

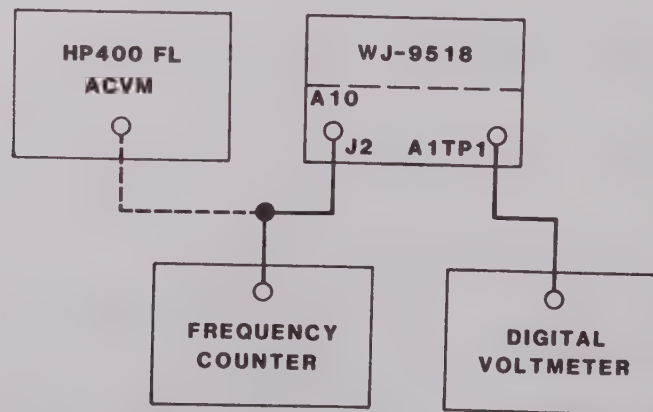


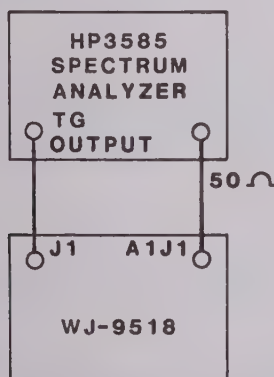
Figure 4-12. 3rd LO Alignment, Equipment Connections

2. With the unit set to the standard test settings listed in **Table 4-3**, observe the displayed frequency on the frequency counter. Ensure FINE TUNING is 0.
3. Adjust C16 until the tuning voltage at TP1 indicates 10.4 Vdc (± 0.5 Vdc).
4. Measure the frequency at J2. It should indicate 500 kHz (± 1 Hz).
5. Tune the FINE TUNE to +50 Hz. The frequency counter should display 500.050 kHz.
6. Tune the FINE TUNE to -50 Hz. The frequency counter should display 499.950 kHz.
7. Disconnect the frequency counter and connect the ACVM to J2. The output level should be 120 mV (± 100 mV).
8. Disconnect all test equipment.

4.7.5

INPUT CONVERTER ALIGNMENT PROCEDURES

1. Connect the test equipment as illustrated in **Figure 4-13** and remove JW1.

**Figure 4-13. Input Converter Equipment Connections****CAUTION**

Do not attempt to align the Input Converter unless the proper test equipment (Refer to **Table 4-1**) is utilized and only after the input filter has been proven to be defective.

2. **Figure 4-14** illustrates a typical Input Converter swept response with the notch frequency and the adjustment for that notch.
3. Adjust C1 for maximum flatness between 0 and 20 MHz. Adjust C4 for a maximum notch at 25 MHz and adjust C7 for a maximum notch at 30 MHz.
4. Verify that interaction between adjustments and installing the module cover does not cause significant deterioration of the swept signal response. Replace JW1.
5. Repeat steps 1 through 4 for each Input Converter.
6. Disconnect the test equipment.

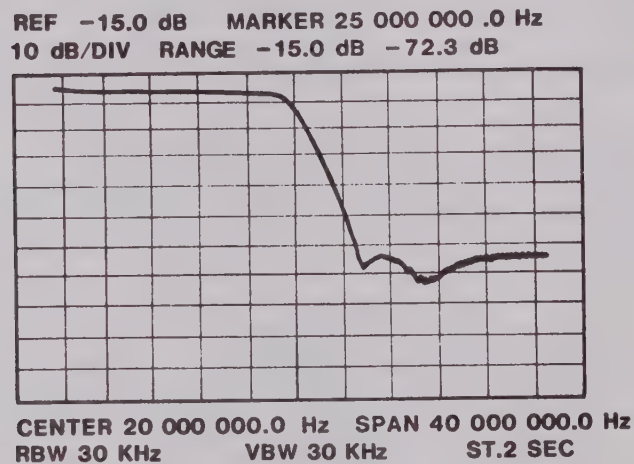


Figure 4-14. Typical Input Converter Swept Response

4.7.6

FREQUENCY CONVERTER ALIGNMENT

1. Connect the test equipment as illustrated in **Figure 4-15** by the solid lines.

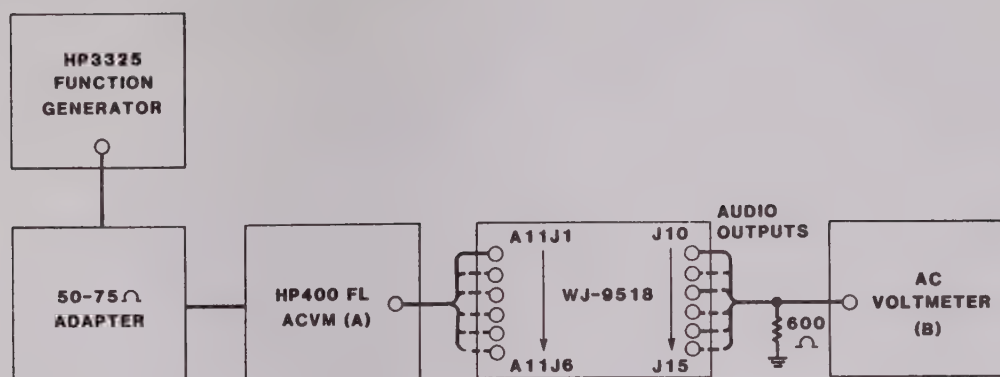


Figure 4-15. Frequency Converter Alignment, Equipment Connections

2. Set the unit to the standard test settings listed in **Table 4-3**, with the exception of no input bridging.
3. Tune the signal generator to 1001 kHz and an output level of -30 dBm as measured on ACVM(A).
4. With DEMOD 1 selected, adjust the associated front panel gain control (NO. 1) to MAX and adjust L2 for a peak audio output signal at the AUDIO OUTPUT connector (A10-A15) for the selected demodulator.
5. Change the function generator output level to -45 dBm and adjust R41 to produce a signal level slightly greater than +13 dBm (1.1-1.2 Vac) as observed on ACVM(B).
6. Adjust the selected demodulator's gain control to MIN and set the function generator output level to -25 dBm.
7. Adjust R5 to produce a reading of less than +11 dB on ACVM(B).
8. Repeat steps 1 through 7 for the other five demodulators (2-6).
9. Disconnect the test equipment.

NOTE

The adjustment of R63 is a factory adjustment. Field adjustment is not advised but may be performed by observing the 500 kHz signal level on a spectrum analyzer display at the audio output and adjusting R63 for minimum LO amplitude.

SECTION V
REPLACEMENT PARTS LIST

SECTION V

REPLACEMENT PARTS LIST

5.1 UNIT NUMBERING METHOD

The unit numbering method of assigning reference designations (electrical symbol numbers) has been used to identify assemblies, subassemblies (and modules) and parts. An example of the unit numbering method follows:

<u>Subassembly Designation</u>	<u>A1</u>	<u>R1</u>	<u>Class and No. of Item</u>
Identify from right to left as:		First (1) resistor (R) of	first (1) subassembly (A)

As shown on the main chassis schematic, components which are an integral part of the main chassis have no subassembly designation.

5.2 REFERENCE DESIGNATION PREFIX

Partial reference designations have been used on the equipment and on the illustrations in this manual. The partial reference designations consist of the class letter(s) and identifying item number. The complete reference designations may be obtained by placing the proper prefix before the partial reference designations. Reference Designation Prefixes are provided on drawings and illustrations in parentheses within the figure titles.

5.3 LIST OF MANUFACTURERS

<u>Mfr. Code</u>	<u>Name and Address</u>	<u>Mfr. Code</u>	<u>Name and Address</u>
00681	Catalyst Research Corp. 1421 Clarkview Road Baltimore, MD 21209	04239	General Electric Company Chemical & Metallurgical Ventures Opn. Magnetic Mtls. Product Sec. Post Office Box 72 Edmore, MI 49928
00779	Amp, Inc. Post Office Box 3608 Harrisburg, PA 17105	04597	Projects Unlimited Inc. 3680 Wyse Road Post Office Box 1426 Dayton, OH 45414
02735	RCA Corporation Solid State Division Route 202 Somerville, NJ 08876	04713	Motorola Inc. Semiconductor Prodcuts Div. 5005 East McDowell Road Phoenix, AR 85008

<u>Mfr. Code</u>	<u>Name and Address</u>	<u>Mfr. Code</u>	<u>Name and Address</u>
05245	Components Corporation 2857 N. Halstead Street Chicago, IL 60657	24355	Analog Devices, Inc. Post Office Box 280 Norwood, MA 02062
06776	Robertson-Nugent, Inc. 800 E. 8th Street Post Office Box 1208 New Albany, IN 47150	25088	Siemens America, Inc. 186 Wood Avenue S. Iselin, NJ 08830
07263	Fairchild Camera & Instrument Corp. Semiconductor Division 464 Ellis Street Mt. View, CA 94040	27014	National Semi-Conductor Corp. 2950 San Ysidro Way Santa Clara, CA 95051
09021	Airco Electronics Bradford, PA	27193	Cutler-Hammer, Inc. Specialty Products Division 402 North 27th Street Milwaukee, WI 53216
13103	Thermalloy Company 2021 W. Valley View Lane Dallas, TX 75234	27956	Relcom 3333 Hillview Avenue Palo Alto, CA 94304
14632	Watkins-Johnson Company CEI Division 700 Quince Orchard Road Gaithersburg, MD 20878	28480	Hewlett-Packard Company Corporate Headquarters 1501 Page Mill Road Palo Alto, CA 94304
17856	Siliconix, Inc. 2201 Laurelwood Road Santa Clara, CA 95050	29990	American Technical Ceramics Division of Phase Industries 1 Norder Lane Huntington Station, NY 11746
18324	Signetics Corporation 811 East Arques Avenue Sunnyvale, CA 94086	33095	Spectrum Control Inc. 152 E. Main Street Fairview, PA 16415
19505	Applied Engineering Products Co. Division of Samarius Inc. 300 Seymour Avenue Derby, CT 06418	34649	Intel Corporation 3585 S.W. 198th Avenue Aloha, OR 97005
22526	Berg Electronics Route 83 New Cumberland, PA 17070	4W715	Linear Technology 1630 McCarthy Blvd. Milpitas, CA 95035

<u>Mfr. Code</u>	<u>Name and Address</u>	<u>Mfr. Code</u>	<u>Name and Address</u>
51642	Centre Engineering Inc. 2820 E. College Avenue State College, PA 16801	75915	Littelfuse, Inc. 800 E. Northwest Highway Des Plaines, IL 60016
52648	Plessy Semiconductors 1641 Kaiser Irvine, CA 92714	80058	Joint Electronic Type Designation System
52673	KSW Electronics Corporation South Bedford Street Burlington, MA	80131	Electronics Ind. Association 2001 Eye Street, N.W. Washington, DC 20006
52689	Hewlett-Packard Company Santa Rosa Division Fountain Grove Parkway Santa Rosa, CA 95401	80294	Bourns, Inc. Instrument Division 6135 Magnolia Avenue Riverside, CA 92506
56289	Sprague Electronics Company Marshall Street North Adams, MA 01247	81073	Grayhill, Inc. 561 Hillgrove Avenue LaGrange, IL 60525
58014	Hitachi Magna-Lock Corp. E Maple Street Post Office Box 816 Big Rapids, MI 49307	81312	Winchester Electronics Litton Industries, Inc. Mainstreet & Hillside Avenue Oakville, CT 06779
70903	Belden Corporation 415 South Kilpatrick Chicago, IL 60644	81349	Military Specifications
71279	Cambridge Thermionic Corp. 445 Concord Avenue Cambridge, MA 92138	82389	Switchcraft, Inc. 5555 North Elston Avenue Chicago, IL 60630
72982	Erie Technological Products Inc. 664 West 12th Street Erie, PA 16512	91293	Johanson, Manufacturing Co. Post Office Box 329 Boonton, NJ 07005
73138	Beckman Instruments Inc. Helipot Division 2500 Harbor Boulevard Fullerton, CA 92634	95104	Collins Radio Company 1200 North Alma Road Richardson, TX 75080
74840	Illinois Capacitor Inc. 3757 W. Toulty Avenue Lincolnwood, IL 60645	95121	Quality Components, Inc. Post Office Box 113 St. Mary', PA 15857

<u>Mfr. Code</u>	<u>Name and Address</u>	<u>Mfr. Code</u>	<u>Name and Address</u>
95146	Alco Electronics Products, Inc. Post Office Box 1348 Lawrence, MA 01842	99800	American Precision Industries Delevan Electronics Division 270 Quaker Road East Aurora, NY 14052
	Sealelectro Corporation 225 Hoyt Mamaroneck, NY 10544		

5.4

PARTS LIST

The parts list which follows contains all electrical parts used in the equipment and certain mechanical parts which are subject to unusual wear or damage. When ordering replacement parts from the Watkins-Johnson Company, specify the type and serial number of the equipment and the reference designation and description of each part ordered. The list of manufacturers provided in paragraph 5.3 and the manufacturer's part number for components are included as a guide to the user of the equipment in the field. These parts may not necessarily agree with the parts installed in the equipment; however, the parts specified in this list will provide satisfactory operation of the equipment. Replacement parts may be obtained from any manufacturer as long as the physical and electrical parameters of the part selected agree with the original indicated part. In the case of components defined by a military or industrial specification, a vendor which can provide the necessary component is suggested as a convenience to the user.

NOTE

As improved semi-conductors become available, it is the policy of Watkins-Johnson to incorporate them in proprietary products. For this reason some transistors, diodes and integrated circuits installed in the equipment may not agree with those specified in the parts lists and schematic diagrams of this manual. However, the semiconductors designated in the manual may be substituted in every case with satisfactory results.

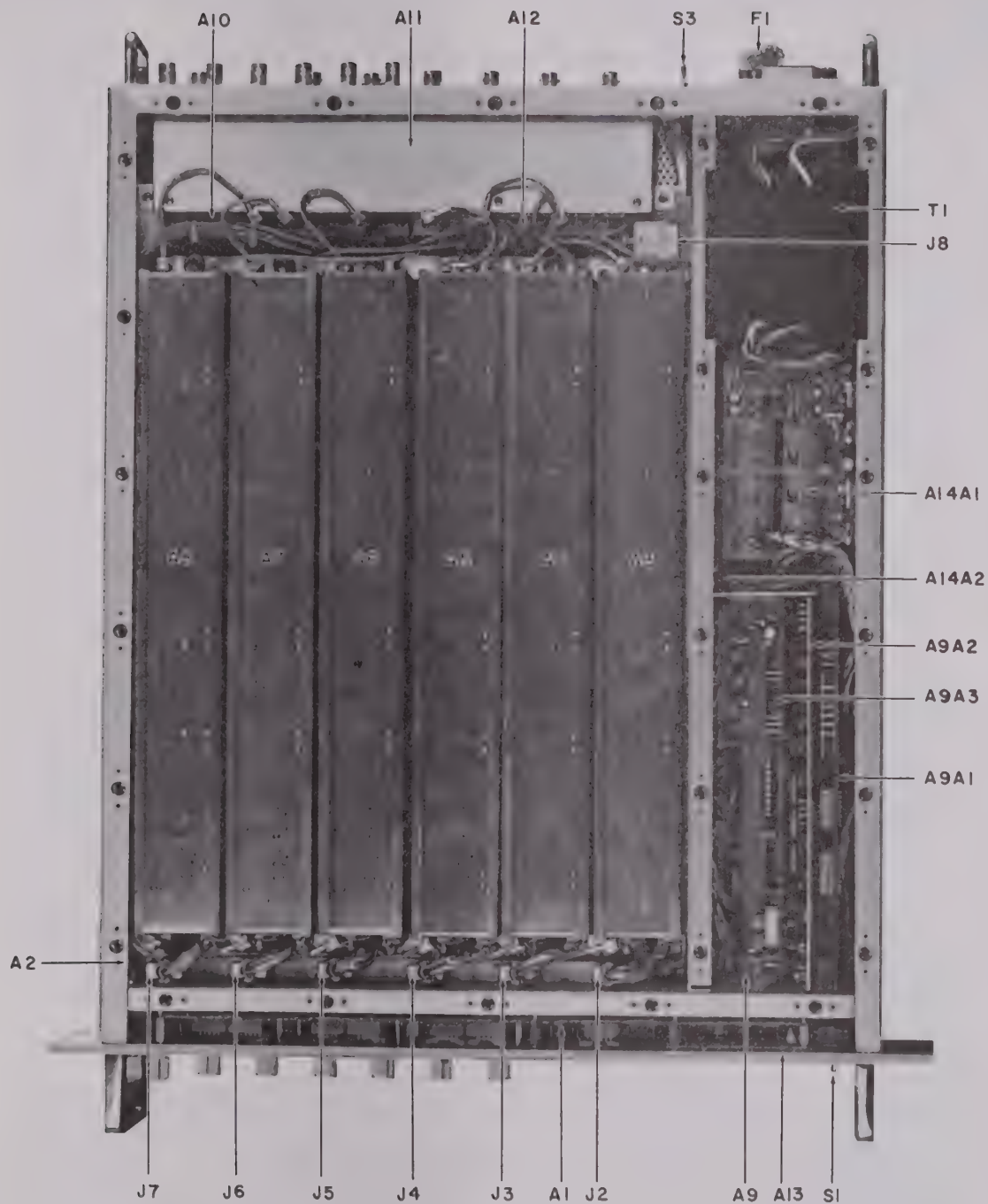


Figure 5-1. WJ-9518BE-9S FDM Demodulator,
Top View, Location of Components

5.5 TYPE WJ-9518BE-9S, MAIN CHASSIS

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	Display	1	796374-1	14632	
A2	Headphone Amplifier	1	796387-1	14632	
A3	Demodulator	6	796381-1	14632	
A4 Thru A8	Same as A3				
A9	Digital Motherboard	1	796375-1	14632	
A10	3rd LO Synthesizer	1	776009-1	14632	
A11	Baseband Amplifier	1	796370-1	14632	
A12	Reference Generator	1	796376-1	14632	
A13	Keyboard	1	796380-1	14632	
A14	Power Supply	1	766013-1	14632	
C1	Not Used				
C2	Capacitor, Ceramic, Disc: 0.022 μ F, 10%, 100 V	1	CK06BX223K	81349	
C3	Not Used				
C4	Capacitor, Ceramic, Feedthru: 5000 pF, 200 V	1	2425-001X5WD-502AA	32897	
C5	Not Used				
C6	Capacitor, Ceramic, Feedthru: 0.05 μ F, 300 V	1	54-785-005-503P	73095	
E1	Terminal	3	AD4A1	92825	
E2	Same as E1				
E3	Same as E1				
FL1J1	Line Filter	1	IEF2	05245	
F1	Fuse Cartridge	1	MDL3/4	71400	
J1	Connector, Receptacle	1	553122-1	00779	
J2	Connector, Receptacle	6	SRE14SNSS	81312	
J3 Thru J7	Same as J7				
J8	Connector, Receptacle	1	SRE9SNSS	81312	
J9	Connector, Phone Jack	1	L11	82389	
J10	Filter Lowpass	6	52-713-301	33095	
J11 Thru J15	Same as J10				
L1	Coil, Fixed, Mold: 6800 μ H, 5%	1	2500-68	99800	
P1	Connector/Receptacle	1	65847-027	22526	
P2	Connector/Plug	1	3-87456-0	00779	
P3	Connector/Receptacle	1	65484-017	22526	
P4	Connector/Receptacle	1	609-4030	15912	
P5	Housing/Connector	1	87456-6	00779	
P6	Connector/Receptacle	1	65484-005	22526	
P7	Connector/Receptacle	1	609-2030	15912	
P8	Connector, Plug	2	3-87456-6	00779	

MAIN CHASSIS

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
P9	Same as P8				
P10	Connector/Jack	20	2002-7571-005	19505	
P11	Same as P10				
P12	Connector/Plug	18	2105-7521-005	19505	
P13 Thru P23	Same as P12				
P24 Thru P26	Same as P10				
P27	Same as P12				
P28 Thru P30	Same as P10				
P31	Same as P12				
P32 Thru P34	Same as P10				
P35	Same as P12				
P36 Thru P38	Same as P10				
P39	Same as P12				
P40 Thru P42	Same as P10				
P43	Same as P12				
P44 Thru P46	Same as P10				
P47	Same as P12				
P48	Same as P5				
P49	Connector/Plug	1	2-87456-0	00779	
R1	Potentiometer, Modified				
R2 Thru R6	Same as R1				
R7	Potentiometer, Modified	1	180401-1	14632	
S1	Switch, Toggle	1	MTA106D	95146	
S2	Switch, Toggle	2	MTA206N	95146	
S3	Same as S1				
W1	Cable Assembly	1	17300-333-1	14632	
W2	Cable Assembly	1	17300-333-2	14632	
W3	Cable Assembly	1	17300-333-3	14632	
W4	Cable Assembly	1	17300-333-4	14632	
W5	Cable Assembly	1	17300-333-5	14632	

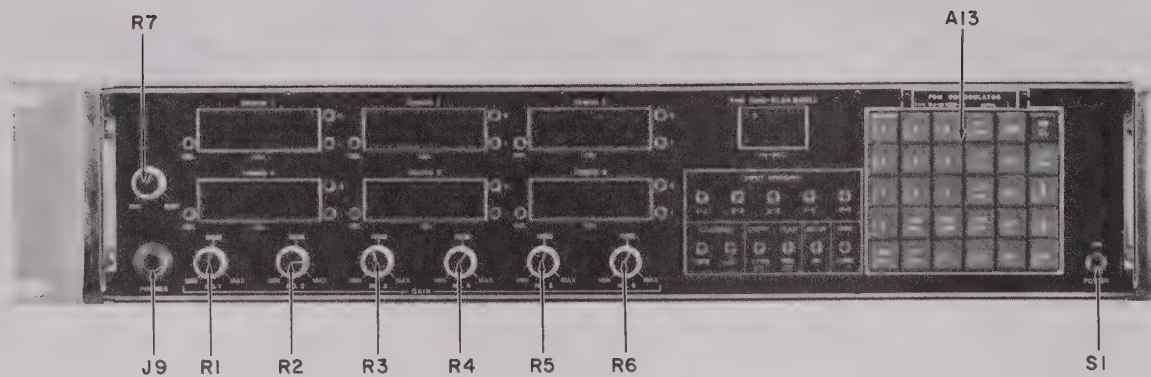


Figure 5-2. WJ-9518BE-9S FDM Demodulator,
Front View, Location of Components



Figure 5-3. WJ-9518BE-9S FDM Demodulator,
Rear View, Location of Components

MAIN CHASSIS

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
W6	Cable Assembly	1	17300-333-6	14632	
W7	Cable Assembly	1	17300-333-7	14632	
W8	Cable Assembly	1	17300-333-8	14632	
W9	Cable Assembly	1	17300-333-9	14632	
W10	Cable Assembly	1	17300-333-10	14632	
W11	Cable Assembly	1	17300-333-11	14632	
W12	Cable Assembly	1	17300-333-12	14632	
W13	Cable Assembly	1	17300-333-13	14632	
W14	Cable Assembly	1	17300-333-14	14632	
W15	Cable Assembly	1	17300-333-15	14632	
W16	Cable Assembly	1	17300-333-16	14632	
W17	Cable Assembly	1	17300-333-17	14632	
W18	Cable Assembly	1	17300-333-18	14632	
W19	Cable Assembly	1	17300-333-19	14632	
W20	Cable Assembly	1	380592-1	14632	
W21	Cable Assembly	1	380592-2	14632	

5.5.1

TYPE 796374-1 DISPLAY

REF DESIG PREFIX A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Electrolytic, Tantalum: 22 μ F, 20%, 10 V	1	196D226X0010JE3	56289	
C2	Capacitor, Ceramic, Disc: 0.1 μ F, 20%, 50 V	2	34475-1	14632	
C3	Capacitor, Electrolytic, Tantalum: 220 μ F, 20%, 10 V	1	196D227X0010TE4	56289	
C4	Same as C3				
C5	Same as C2				
CR1	Diode	29	HLMP-1301	28480	
CR2 Thru CR29	Same as CR1				
D1	Integrated Circuit	13	DL-430M	25088	
D2 Thru D39	Same as D1				
J1	Connector, Receptacle	1	609-4007	15912	
J2	Connector, Receptacle	1	65624-110	22526	
R1	Resistor, Fixed, Film: 33 Ω , 5%, 1/4 W	32	CF 1/4-33 OHMS/J	09021	
R2 Thru R32	Same as R1				
U1	Integrated Circuit	4	UDN2981A	52689	
U2	Integrated Circuit	4	MM74C374N	27014	
U3	Same as U1				
U4	Same as U2				
U5	Same as U1				
U6	Same as U2				
U7	Same as U2				
U8	Same as U1				
U9	Integrated Circuit	1	CD4514BD	02735	
U10	Integrated Circuit	7	ULN-2061M	56289	
U11 Thru U16	Same as U10				

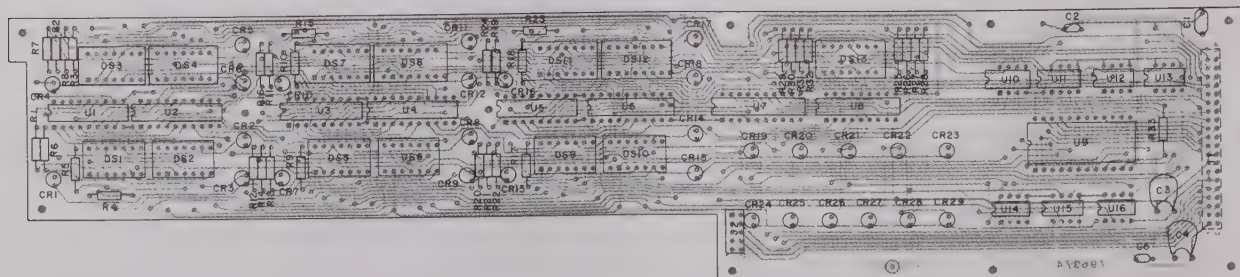


Figure 5-4. Type 796374-1 Display (A1),
Location of Components

5.5.2 TYPE 796387-1 HEADPHONE AMPLIFIER

REF DESIG PREFIX A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Electrolytic, Tantalum: 1.0 μ F, 10%, 35 V	2	CS13BF105K	81349	
C2	Capacitor, Electrolytic, Tantalum: 33 μ F, 10%, 20 V	3	CS13BE336K	81349	
C3	Capacitor, Ceramic, Monolithic: 3300 pF, $\pm$ 2%, 100 V	1	200-100-NPO-332G	51642	
C4	Same as C1				
C5	Capacitor, Electrolytic, Tantalum: 15 μ F, 10%, 20 V	2	C513BE156K	81349	
C6	Same as C2				
R1	Resistor, Fixed, Film: 10 k Ω , 5%, 1/4 W	1	CF 1/4-10K/J	09021	
R2	Resistor, Fixed, Film: 3.3 k Ω , 5%, 1/4 W	2	CF 1/4-3.3K/J	09021	
R3	Resistor, Fixed, Film: 4.7 k Ω , 5%, 1/4 W	1	CF 1/4-4.7K/J	09021	
R4	Resistor, Fixed, Film: 3.9 k Ω , 5%, 1/4 W	1	CF 1/4-3.9K/J	09021	
R5	Same as R2				
R6	Resistor, Fixed, Film: 2.7 Ω , 5%, 1/4 W	2	CF 1/4-2.7 OHMS/J	09021	
R7	Resistor, Fixed, Film: 75 k Ω , 5%, 1/4 W	1	CF 1/4-75K/J	09021	
R8	Resistor, Fixed, Film: 560 Ω , 5%, 1/4 W	1	CF 1/4-560 OHMS/J	09021	
R9	Same as R6				
U1	Integrated Circuit	1	MC3340P	04713	
U2	Integrated Circuit	1	741HC	07263	
E1	Terminal Forked	5	140-1941-02-01	71279	
E2 Thru E5	Same as E1				

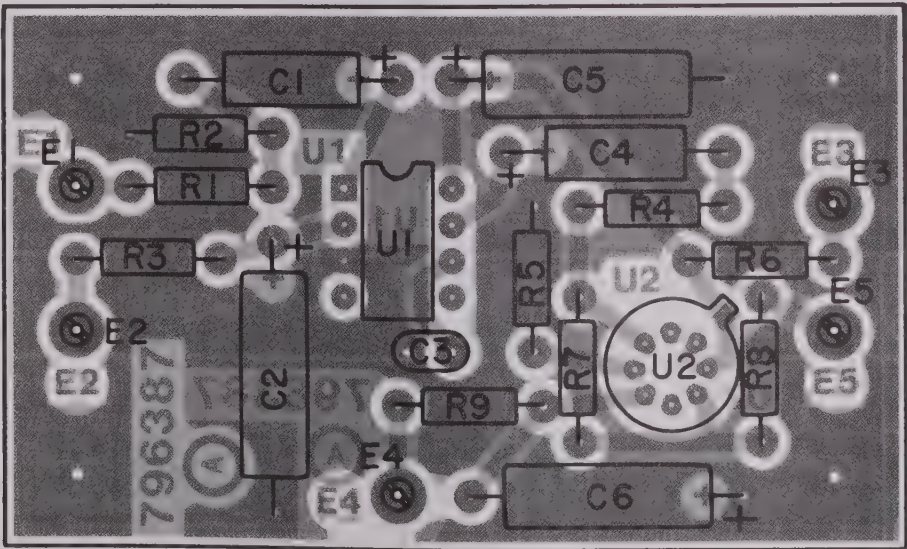


Figure 5-5. Type 796387-1 Headphone Amplifier (A2),
Location of Components

5.5.3

TYPE 796381-1 DEMODULATOR

REF DESIG PREFIX A3-A8

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	Input Converter	1	380712-1	14632	
A2	Frequency Converter	1	380595-1	14632	
A3	1st LO Synthesizer	1	380596-1	14632	
A4	2nd LO Synthesizer	1	380544-1	14632	
E1	Terminal	2	SFU16Y	04013	
FB1	Ferrite Bead	18	56-590-65-4A	02114	
FB2 Thru FB18	Same as FB1				
C1	Capacitor, Ceramic, Feedthru: 1000 pF, GMV, 500 V	7	54-794-009-102W	33095	
C2 Thru C4	Same as C1				
C5	Capacitor, Ceramic, Feedthru: 330 pF, 10%, 500 V	5	54-794-001-3311	33095	
C6 Thru C9	Same as C5				
C10 Thru C12	Same as C1				
J1	Connector, Receptacle	3	2012-1511-000	19505	
J2	Same as J1				
J3	Same as J1				
P1	Connector, Plug	1	SRE14PNSS	81312	

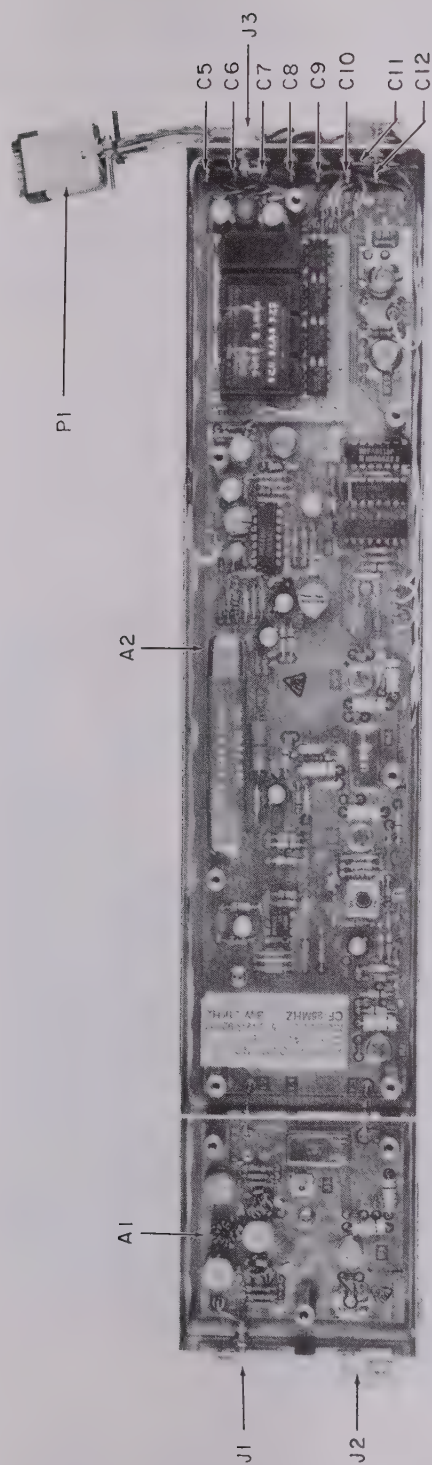


Figure 5-6. Type 796381-1 Demodulator (A3-A8),
Left Side View, Location of Components

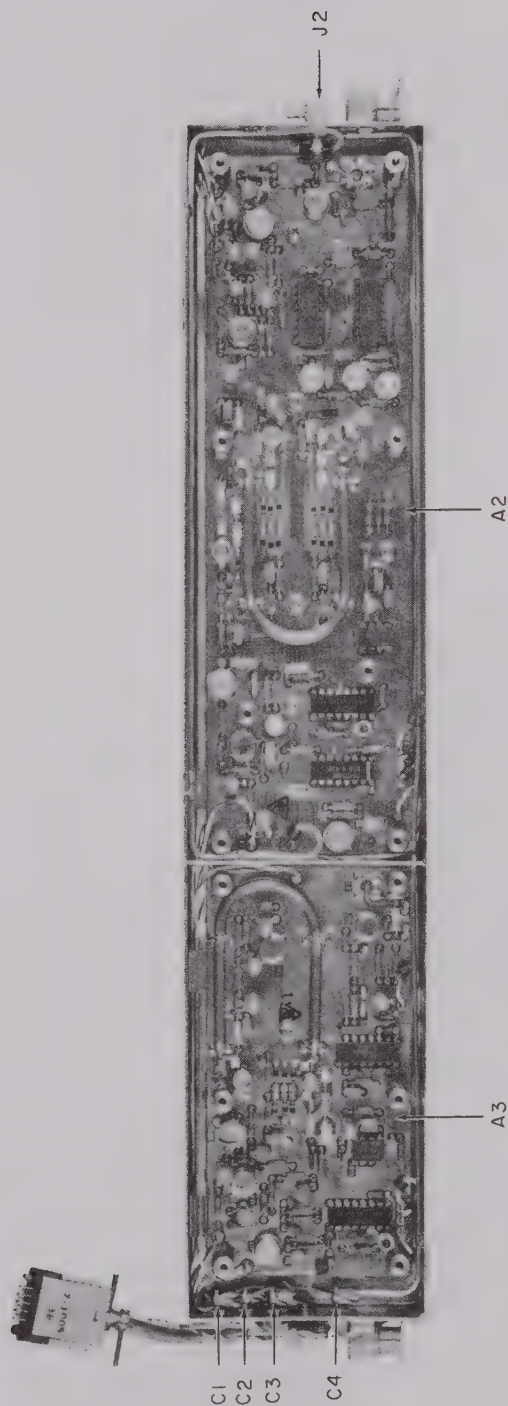


Figure 5-7. Type 796381-1 Demodulator (A3-A8),
Right Side View, Location of Components

5.5.3.1 Part 380712-1 Input Converter

REF DESIG PREFIX A3A1-A8A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Variable, Ceramic: 2-8 pF, 350 V	2	538-011A2-8	72982	
C2	Capacitor, Ceramic, Monolithic: 9.1 pF, ±0.25 pF, 100 V, NPO	1	10-100-NPO-919C	51642	
C3	Capacitor, Ceramic, Monolithic: 130 pF, ±2%, 100 V NPO	1	200-100-NPO-131G	51642	
C4	Capacitor, Ceramic, Monolithic: 5.5-18 pF, 350 V	2	538-011A5.5-18	72982	
C5	Capacitor, Ceramic, Monolithic: 68 pF ±2%, 100 V NPO	1	200-100-NPO-680G	51642	
C6	Capacitor, Ceramic, Monolithic: 270 pF, ±2%, 100 V NPO	1	150-100-NPO-271G	51642	
C7	Same as C4				
C8	Capacitor, Ceramic, Monolithic: 47 pF, ±2%, 100 V NPO	1	150-100-NPO-470G	51642	
C9	Capacitor, Ceramic, Monolithic: 240 pF, ±2%, 100 V NPO	1	150-100-NPO-241G	51642	

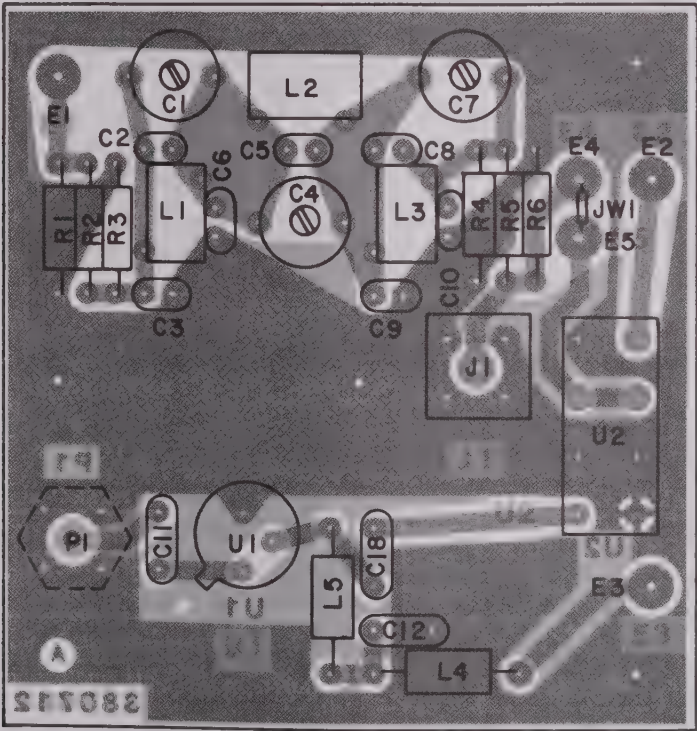


Figure 5-8. Part 380712-1 Input Converter (A3A1-A8A1),
Location of Components

REF DESIG REF A3A1-A8A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C10	Capacitor, Ceramic, Monolithic: 100 pF, $\pm 2\%$, 100 V NPO	1	200-100-NPO-101G	51642	
C11	Capacitor, Ceramic, Disc: 0.01 μ F, 20%, 50 V	13	34453-1	14632	
C12	Same as C11				
C13	Same as C11				
J1	Connector, Receptacle	1	2009-7511-000	19505	
JW1	Wire, Electrolytic, Buss	AR	8020 20 AWE BUSSWIRE	70903	
L1	Coil, Toroidal	1	20681-252	14632	
L2	Coil, Toroidal	1	20681-253	14632	
L3	Coil, Toroidal	1	20681-254	14632	
L4	Coil, Fixed: 15 μ H, 10%	2	1537-40 (14046-6)	99800	
L5	Same as L4				
P1	Connector	1	52-051-000	98291	
R1	Resistor, Fixed, Film: 82.5 Ω , 1%, 1/10 W	2	RN55C82R5F	81349	
R2	Resistor, Fixed, Film: 93.1 k Ω , 1%, 1/10 W	1	RN55C93R1F	81349	
R3	Same as R1				
R4	Resistor, Fixed, Film: 301 k Ω , 1%, 1/10 W	2	RN55C3010F	81349	
R5	Resistor, Fixed, Film: 18.2 k Ω , 1%, 1/10 W	1	RN55D18R2F	81349	
R6	Same as R4				
U1	Integrated Circuit, Amplifier Linear	1	MWA120	04713	
U2	Mixer, Balanced	1	M6D	27956	

5.5.3.2 Part 380595-1 Frequency Converter

REF DESIG PREFIX A3A2-A8A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 0.01 μ F, 20%, 50 V	14	34453-1	14632	
C2 Thru C4	Same as C1				
C5	Capacitor, Ceramic, Disc: 0.47 μ F, 20%, 50 V	2	34452-1	14632	
C6	Capacitor, Ceramic, Monolithic: 36 pF, $\pm$ 2%, 100 V NPO	1	150-100-NPO-360G	51642	
C7	Capacitor, Ceramic, Monolithic: 330 pF, $\pm$ 2%, 100 V NPO	1	150-100-NPO-331G	51642	
C8 Thru C14	Same as C1				
C15	Capacitor, Ceramic, Monolithic: 3600 pF, $\pm$ 2%, 100 V NPO	2	300-100-NPO-362G	51642	
C16	Same as C15				
C17	Same as C1				
C18	Capacitor, Ceramic, Disc: 0.1 μ F, 20%, 50 V	13	34475-1	14632	
C19	Same as C18				
C20	Same as C1				
C21	Capacitor, Ceramic, Disc: 24 pF, 5%, 50 V, NPO	1	8111-050-COGO-240J	72982	
C22	Same as C18				
C23	Same as C18				
C24	Capacitor, Ceramic, Monolithic: 47 pF, $\pm$ 2%, 100 V, NPO	1	150-100-NPO-470G	51642	
C25	Capacitor, Ceramic, Monolithic: 27 pF, $\pm$ 2%, 100 V, NPO	1	150-100-NPO-270G	51642	
C26 Thru C32	Same as C18				
C33	Capacitor, Electrolytic, Tantalum: 4.7 μ F, 20%, 35 V	1	196D475X0035JE3	56289	
C34	Capacitor, Electrolytic, Tantalum: 47 μ F, 20%, 20 V	4	196D476X0020PE4	56289	
C35	Capacitor, Ceramic, Monolithic: 1000 pF, $\pm$ 2%, 100 V, NPO	2	150-100-NPO-102G	51642	
C36	Same as C35				
C37	Same as C18				
C38	Same as C34				
C39	Capacitor, Ceramic, Monolithic: 1000 pF, -2%, 100 V, NPO	1	300-100-NPO-130G	51642	
C40	Capacitor, Ceramic, Monolithic: 2200 pF, $\pm$ 2%, 100 V, NPO	2	200-100-NPO-222G	51642	
C41	Same as C40				
C42	Same as C18				
C43	Same as C1				
C44	Same as C34				
C45	Same as C34				

REF DESIG PREFIX A3A2-A8A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C46	Capacitor, Electrolytic, Tantalum: 220 μ F, 20%, 10 V	1	196D227X0010TE4	56289	
C47	Same as C5				
E1	Terminals	18	220125		
E2 Thru E11	Same as E1				
E12	Not Used				
E13 Thru E19	Same as E1				
FL1	Filter/BP	1	92297	14632	
FL2	Filter/EQL	1	526-8476-020A&B	95104	
L1	Coil, Fixed: 15 μ H, 10%	4	1537-40	99800	
L2	Coil, Variable	1	558-7107-14	71279	
L3	Same as L1				
L4	Same as L1				
L5	Same as L1				
L6	Coil, Fixed: 8.2 μ H, 10 %	1	1537-34	99800	
L7	Coil, Fixed: 3.3 mH, 5%	1	2500-52	99800	
L8	Coil, Fixed, Mold: 1000 μ H, 5%	1	2500-28	99800	
L9	Same as L8				
L10	Coil, Fixed, Mold: 1500 μ H, 5%	1	2500-36	99800	
P1	Connector	2	52-051-000	98291	
P2	Same as P1				
Q1	Transistor	1	841001-2	04713	
Q2	Transistor	3	2N2857	80131	
Q3	Same as Q2				
Q4	Same as Q2				
RT1	Thermistor	1	1DB801J	RODAN	
R1	Resistor, Fixed, Film: 820 Ω , 5%, 1/4 W	1	CF1/4-820 OHMS/J	09021	
R2	Resistor, Fixed, Film: 100 Ω , 5%, 1/4 W	4	CF1/4-100 OHMS/J	09021	
R3	Resistor, Fixed, Film: 2.0 k Ω , 5%, 1/4 W	1	CF1/4-2K/J	09021	
R4	Same as R2				
R5	Resistor, Trimmer, Film: 5 k Ω , 10%, 1/2 W	1	62PR5K	73138	
R6	Resistor, Fixed, Film: 10 k Ω , 1%, 1/10 W	2	RN55C1002F	81349	
R7	Resistor, Fixed, Film: 200 Ω , 5%, 1/4 W	2	CF1/4-200 OHMS/J	09021	
R8	Resistor, Fixed, Film: 56 Ω , 5% 1/4 W	2	CF1/4-56 OHMS/J	09021	
R9	Resistor, Fixed, Film: 100 k Ω , 1%, 1/10 W	1	RN55C1003F	81349	
R10	Same as R6				
R11	Resistor, Fixed, Film: 2.0 k Ω , 1%, 1/10 W	1	RN55C2001F	81349	
R12	Resistor, Fixed, Film: 150 k Ω , 5%, 1/4 W	1	CF1/4-150K/J	09021	
R13	Same as R2				

REF DESIG PREFIX A3A2-A8A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R14	Resistor, Fixed, Film: 12 kΩ, 5%, 1/4 W	1	CF1/4-12K/J	09021	
R15	Resistor, Fixed, Film: 4.7 kΩ, 5%, 1/4 W	1	CF1/4-4.7K/J	09021	
R16	Resistor, Fixed, Film: 20Ω, 5%, 1/4 W	1	CF1/4-22 OHMS/J	09021	
R17	Resistor, Fixed, Film: 39Ω, 5%, 1/4 W	1	CF1/4-39 OHMS/J	09021	
R18	Resistor, Fixed, Film: 270Ω, 5%, 1/4 W	1	CF1/4-270 OHMS/J	09021	
R19	Resistor, Fixed, Film: 220Ω, 5%, 1/4 W	2	CF1/4-220 OHMS/J	09021	
R20	Resistor, Fixed, Film: 24Ω, 5%, 1/4 W	1	CF1/4-24 OHMS/J	09021	
R21	Same as R19				
R22	Same as R7				
R23	Same as R8				
R24	Resistor, Fixed, Film: 47Ω, 5%, 1/4 W	4	CF1/4-47 OHMS/J	09021	
R25	Resistor, Fixed, Film: 10 kΩ, 5%, 1/4 W	2	CF1/4-10K/J	09021	
R26	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/4 W	2	CF1/4-3.3K/J	09021	
R27	Resistor, Fixed, Film: 240Ω, 5%, 1/4 W	1	CF1/4-240 OHMS/J	09021	
R28	Same as R24				
R29	Resistor, Fixed, Film: 2.43 kΩ, 1%, 1/10 W	1	RN55C2431F	81349	
R30	Resistor, Fixed, Film: 51Ω, 5%, 1/4 W	1	CF1/4-51 OHMS/J	09021	
R31	Resistor, Fixed, Film: 3.92Ω, 1%, 1/10 W	4	RN55C3921F	81349	
R32	Same as R31				
R33	Same as R24				
R34	Same as R26				
R35	Same as R24				
R36	Resistor, Fixed, Film: 470Ω, 5%, 1/4 W	1	CF1/4-470 OHMS/J	09021	
R37	Same as R2				
R38	Resistor, Fixed, Film: 2.74Ω, 1%, 1/10 W	4	RN55C2741F	81349	
R39	Same as R38				
R40	Resistor, Fixed, Film: 1.0 k, 1%, 1/10 W	1	RN55C5620F	81349	
R41	Resistor, Trimmer, Film: 1 kΩ, 10%, 1/2 W	1	62PR1K	73138	
R42	Same as R38				
R43	Same as R38				
R44	Resistor, Fixed, Film: 6.81 kΩ, 1%, 1/10 W	1	RN55C6811F	81349	
R45	Same as R31				
R46	Same as R31				
R47	Resistor, Fixed, Film: 13.3 kΩ, 1%, 1/10 W	2	RN55C1332F	81349	
R48	Same as R47				
R49	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/4 W	2	CF1/4-1K/J	09021	
R50	Resistor, Fixed, Film: 562Ω, 1%, 1/10 W	2	RN55C5620F	81349	
R51	Same as R50				
R52	Resistor, Fixed, Film: 4.7 kΩ, 5%, 1/4 W	1	CF1/4-4.7K/J	09021	
R53	Same as R49				

REF DESIG PREFIX A3A2-A8A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R54	Resistor, Fixed, Film: 2.4 k Ω , 5%, 1/4 W	2	CF1/4-2.4K/J	09021	
R55	Resistor, Fixed, Film: 1.5 k Ω , 5%, 1/4 W	1	CF1/4-1.5K/J	09021	
R56	Same as R55				
R57	Resistor, Fixed, Film: 3.0 k Ω , 5%, 1/4 W	1	CF1/4-3K/J	09021	
R58	Resistor, Fixed, Film: 604 Ω , 5%, 1/4 W	2	CF1/4-604 OHMS/J	09021	
R59	Resistor, Fixed, Film: 560 Ω , 5%, 1/4 W	1	CF1/4-560 OHMS/J	09021	
R60	Resistor, Fixed, Film: 3.65 k Ω , 1%, 1/10 W	1	RN55C3651F	81349	
R61	Same as R58				
R62	Same as R25				
R63	Resistor, Fixed, Film: 500 Ω , 10%, 1/2 W	1	62PR500	73138	
U1	Integrated Circuit	2	MWA110	04713	
U2	Integrated Circuit	1	MC1458N	18324	
U3	Same as U1				
U4	Mixer, Balanced	1	M6D	27956	
U5	Integrated Circuit	1	MWA120	04713	
U6	Integrated Circuit	1	MC1408L8	04713	
U7	Integrated Circuit	1	CD4094BE	02735	
U8	Integrated Circuit	1	CD4081BE	04713	
U9	Integrated Circuit	1	MC1496P	04713	
U10	Integrated Circuit	1	LT1007CH	4W715	
U11	Equalizer - Part of FL2		526-8476-020B	95104	
U12	Integrated Circuit	1	DG200BA	17856	
U13	Integrated Circuit	1	MC34001P	04713	
VR1	Diode, Zener: 6.8 V	1	1N754A	80131	

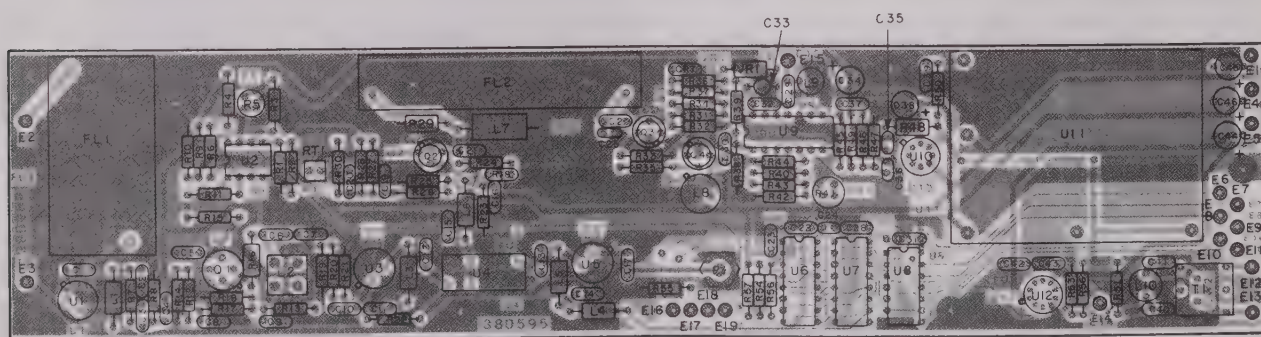


Figure 5-9. Part 380595-1 Frequency Converter (A3A2-A8A2),
Location of Components

5.5.3.3 Part 380596-1 1st LO Synthesizer

REF DESIG PREFIX A3A3-A8A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 470 pF, 10%, 200 V	1	CK05BX471K	81349	
C2	Capacitor, Ceramic, Chip: 4.7 pF, ± 0.1 pF, 500 V	1	ATC100B4R7BP500X	29990	
C3	Capacitor, Ceramic, Chip: 3.3 pF, ± 1 pF, 500 V	2	ATC100B3R3BP500X	29990	
C4	Capacitor, Composition, Tubular: 0.56 pF, 10%, 500 V	1	QC0.56PFK	95121	
C5	Capacitor, Ceramic, Chip: 10 pF, 2%, 500 V	3	ATC100B100GP500X	29990	
C6	Capacitor, Electrolytic, Tantalum: 4.7 μ F, 20%, 35 V	4	196D475X0035JE3	56289	
C7	Not Used				
C8	Capacitor, Ceramic, Disc: 0.1 μ F, 10%, 100 V	2	CK06BX104K	81349	
C9	Same as C8				
C10	Capacitor, Ceramic, Disc: 0.1 μ F, 20%, 50 V	8	34475-1	14632	
C11	Capacitor, Ceramic, Disc: .01 μ F, 20%, 50 V	12	34453-1	14632	
C12	Capacitor, Ceramic, Disc: .15 μ F, 10%, 100 V	3	34452-1	14632	
C13	Same as C10				
C14	Same as C12				
C15	Capacitor, Electrolytic, Tantalum: 4.7 μ F, 20%, 35 V	1	196D475X003SJE3	56289	
C16	Same as C11				
C17	Capacitor, Electrolytic, Tantalum: 18 μ F, 10%, 20 V	7	196D186X9020KE3	56289	
C18	Capacitor, Ceramic, Disc: 220 pF, 10%, 200 V	9	CK05BX221K	81349	
C19	Same as C18				
C20	Same as C12				
C21	Same as C5				
C22 Thru C25	Same as C18				
C26	Same as C3				
C27	Capacitor, Variable, Air: 0.7-6.0 pF, 250 Vdc	2	8050	91293	
C28	Same as C5				
C29	Same as C11				
C30	Same as C11				
C31	Same as C11				
C32	Same as C10				
C33	Same as C11				
C34	Same as C10				
C35	Same as C11				
C36	Same as C11				
C37	Same as C17				
C38	Same as C6				
C39	Same as C18				
C40	Capacitor, Ceramic, Chip: 220 pF, 10%, 500 V	2	ATC100B221KP500X	29990	
C41	Same as C18				
C42	Same as C17				

REF DESIG PREFIX A3A3-A8A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C43	Same as C17				
C44	Capacitor, Ceramic, Disc: .47 μ F, 20%, 50 V	1	34452-1	14632	
C45	Capacitor, Ceramic, Monolithic: 91 pF, $\pm$ 2%, 100 V	2	200-100-NPO-910G	51642	
C46	Capacitor, Ceramic, Monolithic: 160 pF, $\pm$ 2%, 100 V	1	150-100-NPO-161G	51642	
C47	Same as C45				
C48	Same as C11				
C49	Same as C6				
C50	Same as C40				
C51	Same as C3				
C52	Same as C27				
C53	Capacitor, Ceramic, Chip: 22 pF, $\pm$ 2%, 500 V	1	ATC100B220GP500X	29990	
C54	Same as C18				
C55	Same as C11				
C56	Same as C11				
C57	Same as C10				
C58	Same as C6				
C59	Same as C10				
C60	Same as C17				
C61	Same as C10				
C62	Same as C17				
C63	Same as C10				
C64	Same as C17				

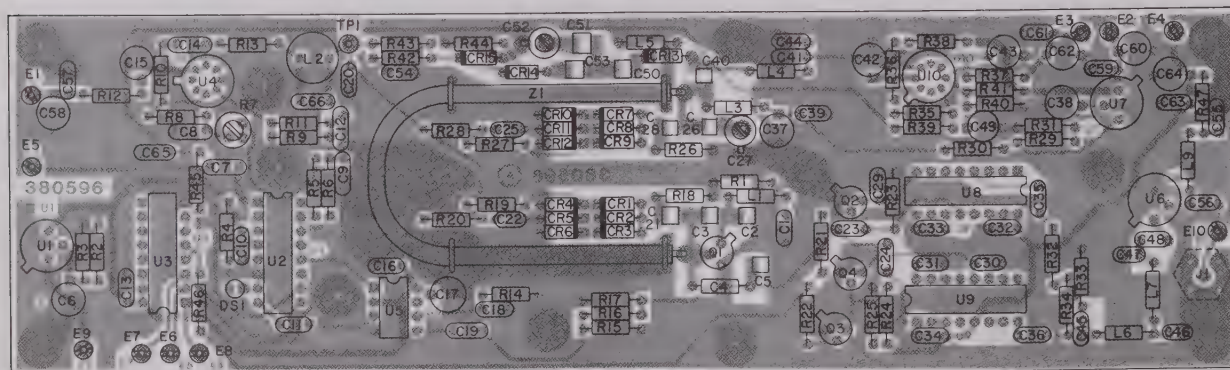


Figure 5-10. Part 380596-1 1st LO Synthesizer (A3A3-A8A3),
Location of Components

REF DESIG PREFIX A3A3-A8A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C65	Same as C11				
C66	Capacitor, Ceramic, Monolithic: 8200 pF, $\pm 2\%$, 100 V	1	300-100-NPO-8226	51642	
CR1	Diode, Varicap	14	KV3901	52673	
CR2 Thru CR12	Same as CR1				
CR13	Diode	1	MPN3401	04713	
CR14	Same as CR1				
CR15	Same as CR1				
DS1	Diode	1	HLMP-1301-1301	28480	
E1	Terminal, Forked	11			
E2 Thru E10	Same as E1				
J1	Connector, Receptacle	1	52-052-0000	98291	
L1	Coil, Fixed, Molded: 0.22 μ F, 10%	1	1025-04	99800	
L2	Coil, Fixed: 47 mH, 10%	1	553-3635-57	71279	
L3	Coil, Fixed, Molded: 0.33 μ H, 10%	1	1025-08	99800	
L4	Coil, Fixed, Molded: 0.39 μ H, 10%	2	1025-10	99800	
L5	Same as L4				
L6	Coil, Fixed, Molded: 0.27 μ H, 10%	2	1025-06	99800	
L7	Same as L6				
Q1	Transistor	1	U310	17856	
Q2	Transistor	3	2N2222A	80131	
Q3	Same as Q2				
Q4	Same as Q2				
R1	Resistor, Fixed, Film: 221 Ω , 1%, 1/10 W	1	RN55C2210F	81349	
R2	Resistor, Fixed, Film: 274 Ω , 1%, 1/10 W	2	RN55C2740F	81349	
R3	Resistor, Fixed, Film: 825 Ω , 1%, 1/10 W	2	RN55C8250F	81349	
R4	Same as R3				
R5	Resistor, Fixed, Film: 750 Ω , 1%, 1/10 W	1	RN55C7500F	81349	
R6	Resistor, Fixed, Film: 1.0 k Ω , 1%, 1/10 W	5	RN55C1001F	81349	
R7	Resistor, Trimmer, Film: 500 Ω , 10%, 1/2 W	1	62PR500	73138	
R8	Same as R6				
R9	Same as R6				
R10	Resistor, Fixed, Film: 15 k Ω , 1%, 1/10 W	4	RN55C1502F	81349	
R11	Same as R10				
R12	Same as R6				
R13	Same as R6				
R14	Resistor, Fixed, Film: 33.2 k Ω , 1%, 1/10 W	2	RN55C3322F	81349	

REF DESIG PREFIX A3A3-A8A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R15	Resistor, Fixed, Film: 150Ω, 1%, 1/10 W	3	RN55C1500F	81349	
R16	Resistor, Fixed, Film: 39.2Ω, 1%, 1/10 W	1	RN55D39R2F	81349	
R17	Same as R15				
R18	Resistor, Fixed, Film: 10 kΩ, 1%, 1/10 W	3	RN55C1002F	81349	
R19	Resistor, Fixed, Film: 8.25 kΩ, 1%, 1/10 W	3	RN55C8251F	81349	
R20	Resistor, Fixed, Film: 2.21 kΩ, 1%, 1/10 W	7	RN55C2211F	81349	
R21	Same as R20				
R22	Same as R21				
R23	Same as R10			81349	
R24	Same as R20				
R25	Same as R10				
R26	Same as R18				
R27	Same as R19				
R28	Same as R20				
R29	Same as R2				
R30	Resistor, Fixed, Film: 100 Ω, 1%, 1/10 W	4	RN55C1000F	81349	
R31	Same as R20				
R32	Resistor, Fixed, Film: 562 Ω, 1%, 1/10 W	2	RN55C5620F	81349	
R33	Same as R15				
R34	Same as R32				
R35	Resistor, Fixed, Film: 392 kΩ, 1%, 1/10 W	1	RN55C3923F	81349	
R36	Resistor, Fixed, Film: 1.5 kΩ, 1%, 1/10 W	1	RN55C1501F	81349	
R37	Same as R30				
R38	Same as R30				
R39	Resistor, Fixed, Film: 4.75 k, 1%, 1/10 W	1	RN55C4751F	81349	
R40	Resistor, Fixed, Film: 6.81 kΩ, 1%, 1/10 W	1	RN55C6811F	81349	
R41	Same as R14				
R42	Same as R19				
R43	Same as R20				
R44	Same as R18				
R45	Same as R30				
R46	Resistor, Fixed, Film: 475Ω, 1%, 1/10 W	1	RN55C4750F	81349	
R47	Resistor, Fixed, Film: 200Ω, 1%, 1/10 W	1	RN55C2000F	81349	
U1	Voltage Regulator	2	LM317H	27014	
U2	Integrated Circuit	1	MC145158P	04713	
U3	Integrated Circuit	1	CD4094BE	02735	
U4	Integrated Circuit	1	LT1007CH	4W715	
U5	Integrated Circuit	1	SP8719B	52648	

REF DESIG PREFIX A3A3-A8A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
U6	Integrated Circuit	1	MWA110	04713	
U7	Same as U1				
U8	Integrated Circuit	1	SP8685B	52648	
U9	Integrated Circuit	1	SP8743B	52648	
U10	Integrated Circuit	1	CA6741T	02735	
Z1	Transmission Line	1	280595-1	14632	

5.5.3.4 Part 380544-1 2nd LO Synthesizer

REF DESIG PREFIX A3A4-A8A4

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Not Used				
C2	Capacitor, Ceramic, Disc: 0.1 μ F, 20%, 50 V	5	34475-1	14632	
C3	Capacitor, Electrolytic, Tantalum: 4.7 μ F, 20%, 35 V	3	196D475X0035JE3	56289	
C4	Capacitor, Ceramic, Disc: .01 μ F, 20%, 50 V	9	34453-1	14632	
C5	Same as C4				
C6	Same as C2				
C7	Same as C3				
C8	Capacitor, Ceramic, Disc: 0.47 μ F, 20%, 50 V	2	34452-1	14632	
C9	Same as C8				
C10	Same as C4				
C11	Capacitor, Electrolytic, Tantalum: 18 μ F, 10%, 20 V	4	196D186X9020KE3	56289	
C12	Same as C4				
C13	Capacitor, Ceramic, Disc: 220 pF, 10%, 200 V	5	CK05BX221K	81349	
C14	Same as C13				
C15	Capacitor, Ceramic, Disc: 1 μ F, 10%, 100 V	1	8131-050-651-105M	72982	
C16	Same as C13				
C17	Capacitor, Ceramic, Chip: 9.1 pF, $\pm$ 0.1 pF, 500 V	1	ATC100B8R2BP500X	29990	
C18	Capacitor, Ceramic, Chip: 2.2 pF, $\pm$ 1 pF, 500 V	1	ATC100B2R2BP500X	29990	

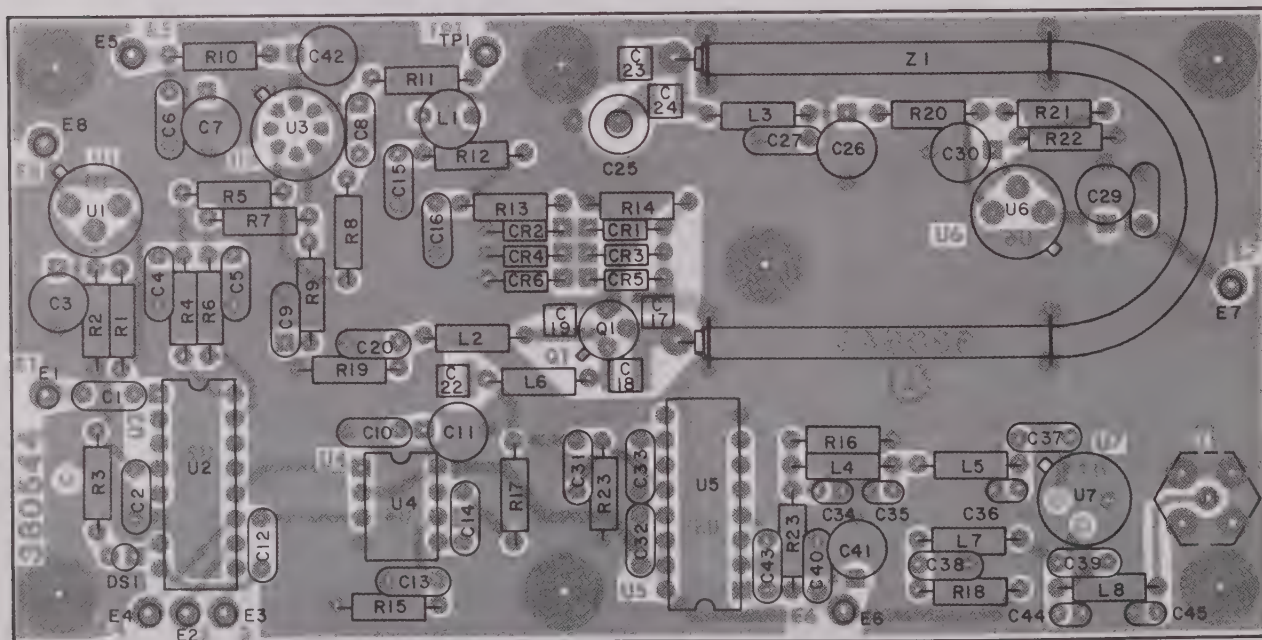


Figure 5-11. Part 380544-1 2nd LO Synthesizer (A3A4-A8A4),
Location of Components

REF DESIG PREFIX A3A4-A8A4

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C19	Capacitor, Ceramic, Chip: 6.8 pF, ± 1 pF, 500 V	1	ATC100B6R8BP500X	29990	
C20	Capacitor, Ceramic, Disc: 470 pF, 10%, 200 V	1	CK05BX471K	81349	
C21	Not Used				
C22	Capacitor, Ceramic, Chip: 10 pF, 2%, 500 V	1	ATC100B100GP500X	29990	
C23	Capacitor, Ceramic, Chip: 43 pF, 2%, 500 V	1	ATC100B430GP500X	29990	
C24	Capacitor, Ceramic, Chip: 22.0 pF, 2%, 500 V	1	ATC100B220GP500X	29990	
C25	Capacitor, Variable, Air: 0.7-6.0 pF, 250 Vdc	1	8050	91293	
C26	Same as C11				
C27	Same as C13				
C28	Same as C2				
C29	Same as C11				
C30	Same as C3				
C31	Same as C13				
C32	Same as C2				
C33	Same as C4				
C34	Capacitor, Electrolytic, Monolithic: 150 pF, $\pm 2\%$, 100 V	4	150-100-NPO-151G	51642	
C35	Capacitor, Ceramic, Monolithic: 240 pF, $\pm 1\%$, 100 V	1	150-100-NPO-241G	51642	
C36	Same as C34				
C37	Same as C4				
C38	Same as C4				
C39	Same as C4				
C40	Same as C2				
C41	Same as C11				
C42	Capacitor, Ceramic, Tantalum: 4.7 μ F, 20%, 35 V	1	196D475X0035JE3	56289	
C43	Same as C4				
C44	Same as C34				
C45	Same as C34				
CR1	Diode, Varicap	6	KV3801	52673	
CR2 Thru CR6	Same as CR1				
DS1	Diode	1	HLMP-1301	28480	
J1	Connector	1	52--052-000	98291	
L1	Coil, Fixed: 15 mH, 10%	1	553-3635-51	71279	
L2	Coil, Fixed, Molded: 0.33 μ H, 10%	2	1025-08	99800	
L3	Same as L2				
L4	Coil, Fixed, Molded: 0.47 μ H, 10%	2	1025-12	99800	
L5	Same as L4				
L6	Coil, Fixed, Molded: 0.1 μ H, 10%	1	1025-94	99800	
L7	Coil, Fixed, Molded: 3.3 μ H, 10%	1	1025-32	99800	
L8	Coil, Fixed, Molded: 0.39 μ H, 10%	1	1025-10	99800	

REF DESIG PREFIX A3A4-A8A4

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
Q1	Transistor	1	U310	17856	
R1	Resistor, Fixed, Film: 274 Ω , 1%, 1/10 W	3	RN55C2740F	81349	
R2	Resistor, Fixed, Film: 825 Ω , 1%, 1/10 W	2	RN55C8250F	81349	
R3	Same as R2				
R4	Resistor, Fixed, Film: 1.0 k Ω , 1%, 1/10 W	6	RN55C1001F	81349	
R5	Same as R4				
R6	Same as R4				
R7	Same as R4				
R8	Resistor, Fixed, Film: 6.81 k Ω , 1%, 1/10 W	2	RN55C6811F	81349	
R9	Same as R8				
R10	Same as R4				
R11	Same as R4				
R12	Resistor, Fixed, Film: 2.21 k Ω , 1%, 1/10 W	2	RN55C2211F	81349	
R13	Resistor, Fixed, Film: 8.25 k Ω , 1%, 1/10 W	1	RN55C8251F	81349	
R14	Resistor, Fixed, Film: 10 k Ω , 1%, 1/10 W	1	RN55C1002F	81349	
R15	Resistor, Fixed, Film: 33.2 k Ω , 1%, 1/10 W	1	RN55C3322F	81349	
R16	Resistor, Fixed, Film: 56.2 k Ω , 1%, 1/10 W	1	RN55C5622F	81349	
R17	Resistor, Fixed, Film: 39.2 k Ω , 1%, 1/10 W	1	RN55C3922F	81349	
R18	Resistor, Fixed, Film: 200 Ω , 1%, 1/10 W	1	RN55C2000F	81349	
R19	Resistor, Fixed, Film: 221 Ω , 1%, 1/10 W	1	RN55C2210F	81349	
R20	Resistor, Fixed, Film: 100 Ω , 1%, 1/10 W	1	RN55C1000F	81349	
R21	Same as R1				
R22	Same as R12				
R23	Resistor, Fixed, Film: 15 k Ω , 1%, 1/10 W	1	RN55C1502F	81349	
R24	Same as R1				
U1	Voltage Regulator	2	LM317H	27014	
U2	Integrated Circuit	1	MC145158P	04713	
U3	Integrated Circuit	1	LT1007CH	4W715	
U4	Integrated Circuit	1	SP8719B	52648	
U5	Integrated Circuit	1	SP8685B	52648	
U6	Same as U1				
U7	Integrated Circuit	1	MWA110	04713	
Z1	Transmission Line	1	280654-1	14632	

5.5.4 TYPE 796375-1 DIGITAL MOTHERBOARD

REF DESIG PREFIX A9

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	Microprocessor	1	796371-1	14632	
A2	IEEE Interface	1	796373-1	14632	
A3	Interface	1	796372-1	14632	
C1	Capacitor, Ceramic, Monolithic: 1000 pF, $\pm 2\%$, 100 V, NPO	18	150-100-NPO-102G	51642	
C2	Capacitor, Ceramic, Disc: 0.1 μ F, 20%, 50 V	9	34475-1	14632	
C3	Not Used				
C4	Capacitor, Electrolytic, Tantalum: 220 μ F, 20%, 10 V	3	196D227X0010TE4	56289	
C5	Same as C1				
C6	Same as C2				
C7	Capacitor, Electrolytic, Tantalum: 4.7 μ F, 20%, 35 V	5	196D475X0035JE3	56289	
C8	Capacitor, Electrolytic, Tantalum: 100 μ F, 20%, 20 V	2	196D107X0020TE4	56289	
C9	Same as C1				
C10	Same as C2				
C11	Same as C7				
C12	Same as C8				
C13	Same as C1				
C14	Same as C2				
C15	Same as C7				
C16	Not Used				
C17	Same as C1				
C18	Same as C2				
C19	Same as C3				
C20	Same as C4				
C21 Thru C33	Same as C1				
C34	Same as C7				
C35	Same as C2				
C36	Same as C2				
C37	Capacitor, Electrolytic, Tantalum: 22 μ F, 20%, 10 V	1	196D226X0010JE3	56289	
C38	Same as C7				
C39	Same as C2				
C40	Same as C2				
C41	Not Used				
C42	Same as C4				
XA9A1A	Header	3	67273-020	22526	
XA9A2A	Same as XA9A1A				
XA9A3A	Same as XA9A1A				
XA9A3B	Header Assembly	1	67273-025	22526	

REF DESIG PREFIX A9

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
J1	Connector, Receptacle	3	65610-140	22526	
J2	Same as J1				
J3	Connector, Receptacle	1	65610-120	22526	
J4	Same as J1				
J5	Connector, Receptacle	1	65610-134	22526	
R1	Resistor, Fixed, Film: 4.7 k Ω , 5%, 1/4 W	12	CF1/4-4.7K/J	09021	
R2 Thru R12	Same as R1				
U1	Integrated Circuit	2	MM74C922N	27014	
U2	Same as U1				

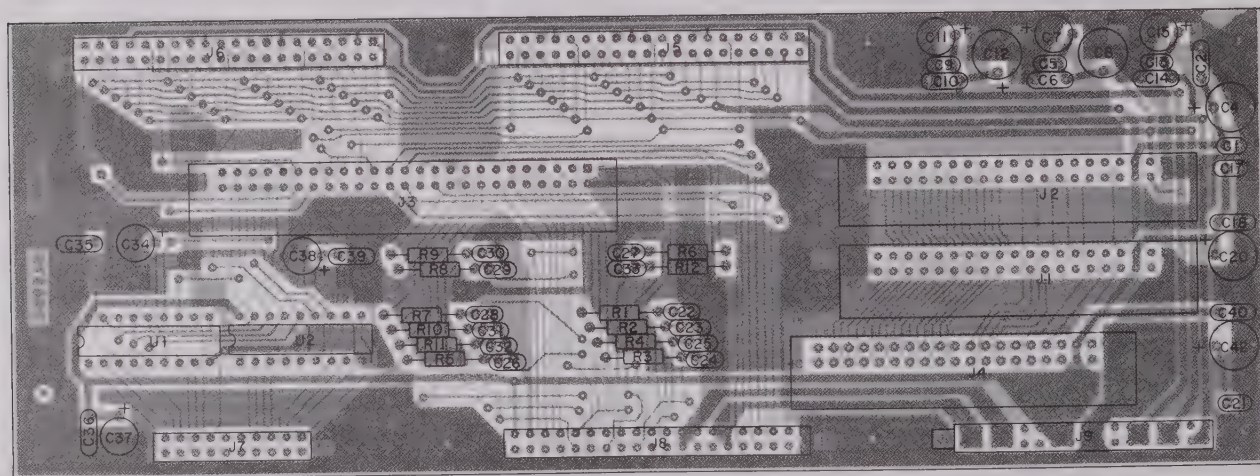


Figure 5-12. Type 796375-1 Digital Motherboard (A9),
Location of Components

5.5.4.1 Type 796371-1 Microprocessor

REF DESIG PREFIX A9A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
BT1	Battery	1	1935	00681	
C1	Capacitor, Ceramic, Monolithic: 20 pF, $\pm 5\%$, 100 V, NPO	1	100-100-NPO-200J	51642	
C2	Capacitor, Ceramic, Monolithic: 33 pF, $\pm 2\%$, 100 V, NPO	1	150-100-NPO-330G	51642	
C3	Capacitor, Ceramic, Disc: 0.1 μ F, 20%, 50 V	11	34475-1	14632	
C4 Thru C7	Same as C3				
C8	Not Used				
C9 Thru C13	Same as C3				
C14	Capacitor, Electrolytic, Tantalum: 100 μ F, 20%, 20 V	1	196D107X0020TE4	56289	
C15	Same as C3				
C16	Capacitor, Ceramic, Monolithic: 100 pF, $\pm 2\%$, 100 V NPO	1	200-100-NPO-101G	51642	
C17	Capacitor, Electrolytic, Tantalum: 47 μ F, 20%, 20 V	1	196D476X0020PE4	56289	
CR1	Diode	1	1N4444	80131	
CR2	Diode	1	5082-2800	28480	
P1	Connector, Receptacle	1	1-102585-2	00779	
Q1	Transistor	2	2N4403	80131	
Q2	Same as Q1				
Q3	Transistor	1	2N4401	80131	
R1	Resistor, Fixed, Film: 1.0M Ω , 5%, 1/8 W	1	CF 1/8-1M/J	09021	
R2	Resistor, Fixed, Film: 1.0 k Ω , 5%, 1/8 W	2	CF 1/8-1.0K/J	09021	
R3	Resistor, Fixed, Film: 22 k Ω , 5%, 1/8 W	3	CF 1/8-22K/J	09021	
R4	Resistor, Fixed, Film: 1.2M Ω , 5%, 1/8 W	1	CF1/8-1.2M/J		
R5	Resistor, Trimmer, Film: 1 k Ω , 10%, 3/4 W	1	89PR1K	73138	
R6	Resistor, Fixed, Film: 4.7 k Ω , 5%, 1/8 W	1	CF 1/8-4.7K/J	09021	
R7	Resistor, Fixed, Film: 470 Ω , 5%, 1/8 W	1	CF 1/8-470 OHMS/J	09021	
R8	Same as R3				
R9	Resistor, Fixed, Film: 100 k Ω , 5%, 1/8 W	1	CF 1/8-100K/J	09021	
R10	Resistor, Fixed, Film: 2.2 k Ω , 5%, 1/8 W	1	CF1/8-2.2K/J	09021	
R11	Resistor, Fixed, Film: 47 k Ω , 5%, 1/8 W	1	CF1/8-47K/J	09021	
R12	Same as R3				
R13	Same as R2				
U1	Integrated Circuit	1	NSC800N-4	27014	
U2	Integrated Circuit	1	MM74HC373N	27014	
U3	Dip Switch	1	1-435704-0	00779	
U4	Integrated Circuit	4	2764	34649	

REF DESIG PREFIX A9A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
U5	Same as U4				
U6	Same as U4				
U7	Not Used				
U8	Integrated Circuit	4	HM6116LP-2	58014	
U9	Integrated Circuit	1	MM74HC244N	27014	
U10	Same as U8				
U11	Same as U8				
U12	Integrated Circuit	1	MM74HC138N	27014	
U13	Integrated Circuit	1	MM74HC32N	27014	
U14	Integrated Circuit	1	CD4093BE	02735	
U15	Resistor, Network	3	765-1-R22K	73138	
U16	Same as U15				
U17	Same as U15				
VR1	Diode, Zener: 3.9 V	1	1N748A	80131	
Y1	Crystal 6.144 MHz	1	E614	72982	

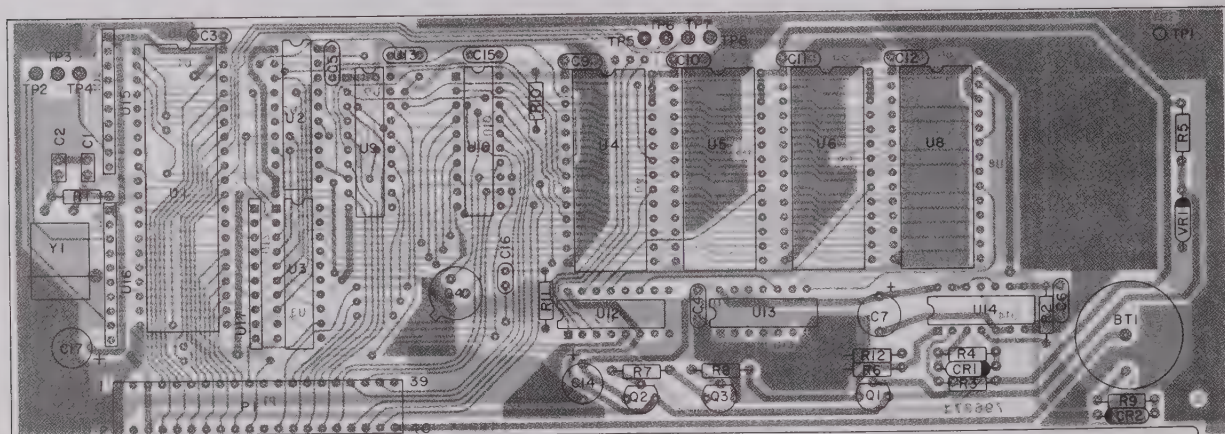


Figure 5-13. Type 796371-1 Microprocessor (A9A1),
Location of Components

5.5.4.2 Type 796373-1 IEEE-488 Interface

REF DESIG PREFIX A9A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 0.1 μ F, 20%, 50 V	5	34475-1	14632	
C2 Thru C5	Same as C1				
C6	Capacitor, Electrolytic, Tantalum: 22 μ F, 20%, 10 V	1	196D226X0010JE3	56289	
E1	Terminal, Forked	9	140-1941-02-01	71279	
E2 Thru E9	Same as E1				
J1	Connector	1	65496-013	22526	
P1	Connector, Receptacle	1	1-102585-2	00779	
R1	Resistor, Fixed, Film: 100 k Ω , 5%, 1/4 W	1	CF 1/4-100K/J	09021	
S1	Switch, DIP	2	76PSB08S	81073	
S2	Same as S1				
U1	Integrated Circuit	1	841137-1	14632	
U2	Integrated Circuit	1	841137-2	14632	
U3	Integrated Circuit	1	P8291A	34649	
U4	Integrated Circuit	2	MM74HC373N	27014	
U5	Same as U4				
U6	Resistor, Network	2	4310R-101-104	80294	
U7	Same as U6				
U8	Integrated Circuit	2	MM74HC138N	27014	
U9	Same as U8				

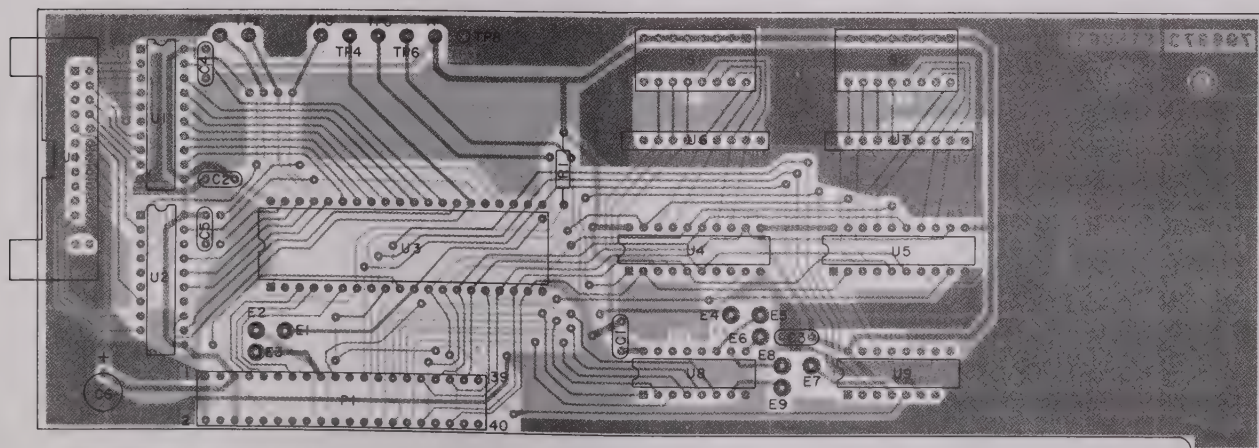


Figure 5-14. Type 796373-1 IEEE-488 Interface (A9A2),
Location of Components

5.5.4.3 Type 796372-1 Interface

REF DESIG PREFIX A9A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Electrolytic, Tantalum: 1 μ F, 20%, 35 V	2	196D105X0035HE3	56289	
C2	Capacitor, Ceramic, Disc: 0.1 μ F, 20%, 50 V	6	34475-1	14632	
C3	Capacitor, Ceramic, Disc: 0.47 μ F, 20%, 50 V	1	34452-1	14632	
C4	Not Used				
C5	Same as C2				
C6	Capacitor, Electrolytic, Tantalum: 22 μ F, 20%, 10 V	2	196D226X0010JE3	56289	
C7	Capacitor, Ceramic, Monolithic: 100 pF, $\pm$ 2%, 100 V, NPO	1	200-100-NPO-101G	51642	
C8					
9	Same as C2				
C10	Same as C2				
C11	Capacitor, Ceramic, Disc: 0.01 μ F, 20%, 50 V	1	34453-1	14632	
C12	Same as C6				
C13	Same as C1				
C14	Same as C2				
LS1	Alarm	1	AT-20	04597	
P1	Connector, Receptacle	1	66527-020	22526	
P2	Receptacle Assembly	1	66527-025	22526	
R1	Resistor, Fixed, Film: 470 k Ω , 5%, 1/8 W	1	CF 1/8-470K/J	09021	
R2	Resistor, Fixed, Film: 10 k Ω , 1%, 1/10 W	2	RN55C1002F	81349	
R3	Same as R2				
R4	Resistor, Fixed, Film: 20 k Ω , 1%, 1/10 W	1	RN55C2002F	81349	
R5	Resistor, Fixed, Film: 150 k Ω , 5%, 1/8 W	1	CF 1/8-150K/J	09021	
R6	Resistor, Fixed, Film: 10 k Ω , 5%, 1/8 W	3	CF 1/8-10K/J	09021	
R7	Same as R6				
R8	Same as R6				
R9	Resistor, Fixed, Film: 47 k Ω , 5%, 1/8 W	1	CF 1/8-47K/J	09021	
R10	Resistor, Trimmer, Film: 50 k Ω , 10%, 1/2 W	1	62PAR100K	73138	
R11	Resistor, Fixed, Film: 2.2 k Ω , 5%, 1/8 W	1	CF 1/8-2.2K/J	09021	
U1	Integrated Circuit	1	CD4013BE	02735	
U2	Integrated Circuit	2	MM74HC373N	27014	
U3	Integrated Circuit	2	MM74HC374N	27014	
U4	Same as U3				
U5	Integrated Circuit	1	MM74HC123N	27014	
U6	Integrated Circuit	2	MM74HC138N	27014	
U7	Integrated Circuit	1	CD4051BE	02735	
U8	Integrated Circuit	1	AD7574JN	24355	
U9	Same as U2				
U10	Integrated Circuit	1	MC1458N	18324	
U11	Integrated Circuit	1	MM74HC32N	27014	
U12	Integrated Circuit	1	MM74HC10N	27014	

REF DESIG PREFIX A9A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
U13	Integrated Circuit	1	MM74HC04N	27014	
U14	Integrated Circuit	1	MM74HC74N	27014	
U15	Integrated Circuit	2	CD4040BE	02735	
U16	Same as U6				
U17	Same as U15				
U18	Integrated Circuit	2	MM74HC157N	27014	
U19	Same as U18				
U20	Integrated Circuit	1	HM6116LP-2	58014	
U21	Integrated Circuit	1	MM74HC245N	27014	

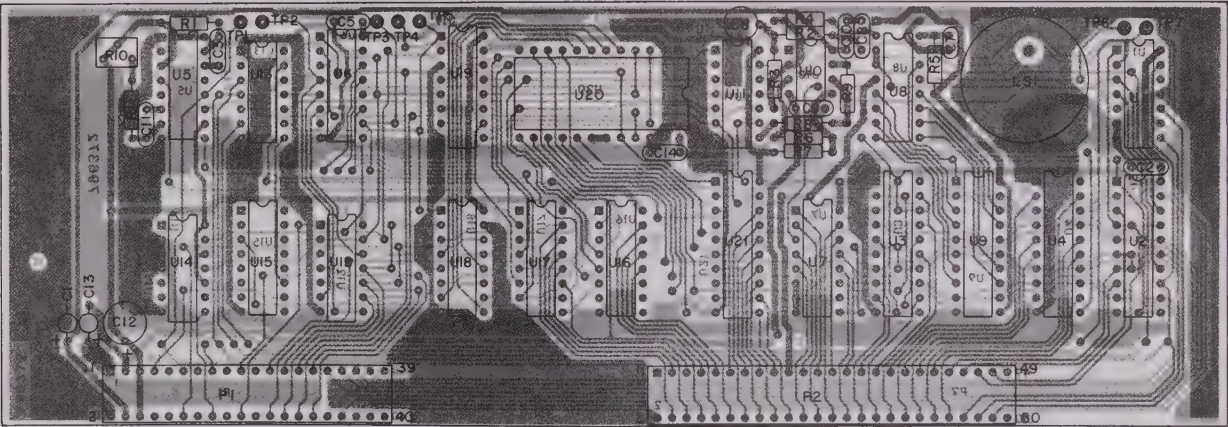


Figure 5-15. Type 796372-1 Interface (A9A3),
Location of Components

5.5.5 TYPE 776009-1 3rd LO SYNTHESIZER		REF DESIG PREFIX A10			
REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	3rd LO Synthesizer Assembly	1	380577-1	14632	
C1	Capacitor, Ceramic, Feedthru: 0.05 μ F, 300 V	3	54-785-002-503P	33095	
C2	Same as C1				
C3	Same as C1				
C4	Not Used				
C5	Capacitor, Ceramic, Feedthru: 33 pF, 10%, 500 V	4	54-794-001-3301	33095	
C6	Same as C5				
C7	Same as C5				
C8	Same as C5				
J1	Connector, Receptacle	7	2004-7511-000	19505	
J2 Thru J7	Same as J1				

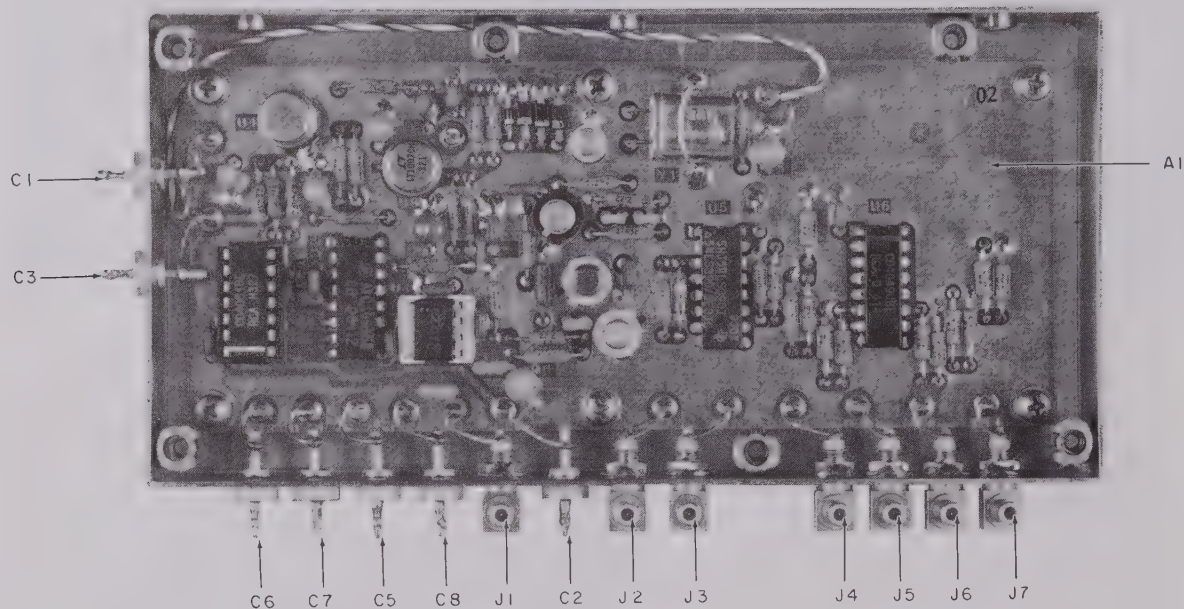


Figure 5-16. Type 776009-1 3rd LO Synthesizer (A10),
Location of Components

5.5.5.1 Part 380577-1 3rd LO Synthesizer Assembly

REF DESIG PREFIX A10A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Electrolytic, Tantalum: 22 μ F, 20%, 10 V	3	196D226X0010JE3	56289	
C2	Capacitor, Ceramic, Disc: 0.01 μ F, 20%, 50 V	2	34453-1	14632	
C3	Capacitor, Ceramic, Disc: 1 μ F, 20%, 50 V	10	34475-1	14632	
C4	Capacitor, Electrolytic, Tantalum: 4.7 μ F, 20%, 35 V	1	196D475X0035JE3	56289	
C5	Same as C1				
C6	Same as C1				
C7	Capacitor, Electrolytic, Tantalum: 3.3 μ F, 20%, 35 V	2	196D335X0035JE3	56289	
C8	Capacitor, Electrolytic, Tantalum: 4.7 μ F, 20%, 35 V	1	196D186X9020KE3	56289	
C9	Same as C7				
C10	Same as C3				
C11	Same as C3				
C12	Same as C3				
C13	Same as C2				
C14	Same as C3				
C15	Same as C3				
C16	Capacitor, Variable, Air: 0-7-6.0 pF, 250 V	1	8050	91293	
C17	Same as C3				
C18	Ceramic, Electrolytic, Tantalum: 18 μ F, 10%, 20 V	1	196D186X9020KE3	56289	
C19	Capacitor, Ceramic, Monolithic: 220 pF, $\pm$ 2%, 100 V	2	150-100-NPO-221G	51642	
C20	Same as C19				
C21	Capacitor, Ceramic, Monolithic: 3300 pF, $\pm$ 2%, 100 V, NPO	1	200-100-NPO-332G	51642	
C22	Same as C3				
C23	Same as C3				
C24	Same as C3				
CR1	Diode	1	U11-3102	52673	
CR2	Diode, Varicap	3	KV3901	52673	
CR3	Same as CR2				
CR4	Same as CR2				
DS1	Diode	1	HLMP-1301	28480	
E1	Terminal, Forked	18	140-1941-02-01	71279	
E2 Thru E18	Same as E1				
L1	Coil, Fixed: 33 μ H, 10%	1	1025-56 (75085-1)	99800	
Q1	Transistor	1	2N2857	80131	
Q2	Transistor	2	2N2222A	80131	
Q3	Same as Q2				
R1	Resistor, Fixed, Film: 274 Ω , 1%, 1/10 W	1	RN55C2740F	81349	
R2	Resistor, Fixed, Film: 825 Ω , 1%, 1/10 W	2	RN55C8250F	81349	

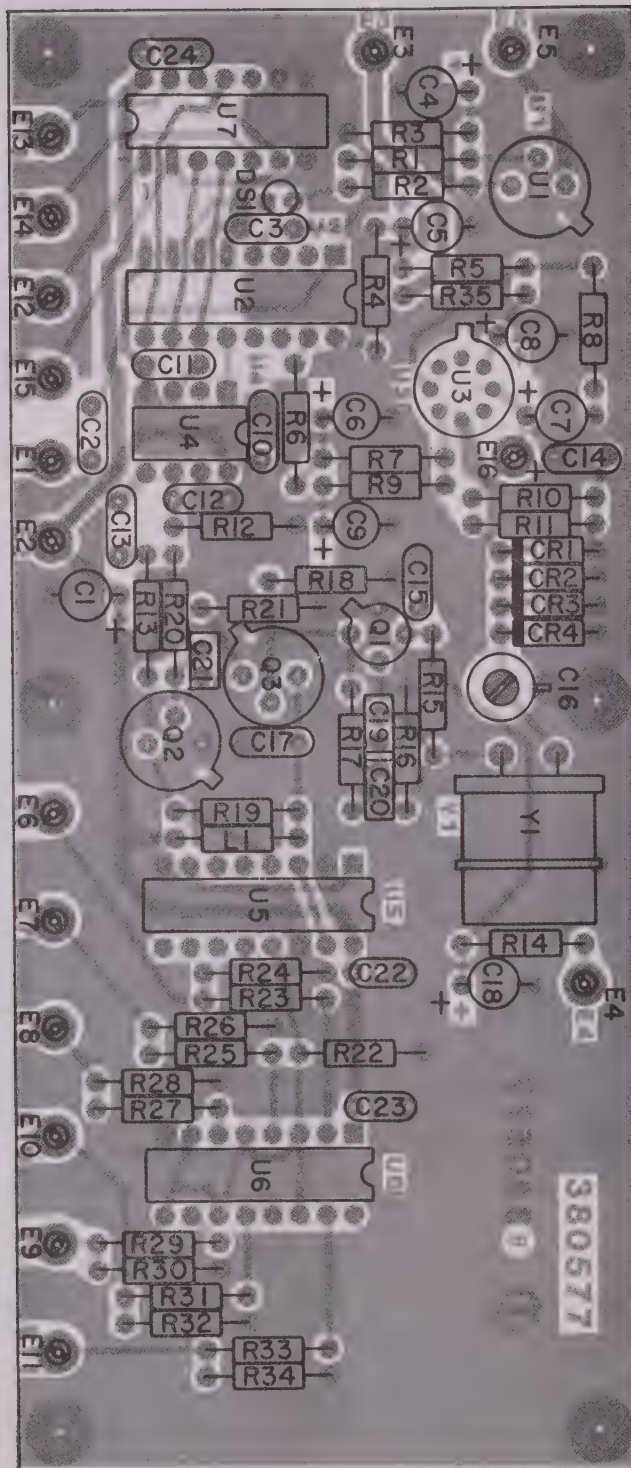


Figure 5-17. Part 380577-1 3rd LO Synthesizer Assembly (A10A1),
Location of Components

REF DESIG PREFIX A10A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R3	Same as R2				
R4	Resistor, Fixed, Film: 1.0 k Ω , 1%, 1/10 W	7	RN55C1001F	81349	
R5	Same as R4				
R6	Same as R4				
R7	Same as R4				
R8	Resistor, Fixed, Film: 475 k Ω , 1%, 1/10 W	2	RN55C4753F	81349	
R9	Same as R8				
R10	Same as R4				
R11	Resistor, Fixed, Film: 22.1 k Ω , 1%, 1/10 W	3	RN55C2212F	81349	
R12	Resistor, Fixed, Film: 33.2 k Ω , 1%, 1/10 W	1	RN55C3322F	81349	
R13	Resistor, Fixed, Film: 100 Ω , 1%, 1/10 W	1	RN55C1000F	81349	
R14	Resistor, Fixed, Film: 2.74 k Ω , 1%, 1/10 W	7	RN55C2741F	81349	
R15	Resistor, Fixed, Film: 68.1 k Ω , 1%, 1/10 W	1	RN55C6812F	81349	
R16	Same as R11				
R17	Resistor, Fixed, Film: 47.5 Ω , 1%, 1/10 W	1	RN55C47R5F	81349	
R18	Same as R4				
R19	Resistor, Fixed, Film: 511 Ω , 1%, 1/10 W	1	RN55C5110F	81349	
R20	Same as R11				
R21	Resistor, Fixed, Film: 681 Ω , 1%, 1/10 W	1	RN55C6810F	81349	
R22	Resistor, Fixed, Film: 2.21 k Ω , 1%, 1/10 W	1	RN55C2211F	81349	
R23	Same as R14				
R24	Resistor, Fixed, Film: 200 Ω , 1%, 1/10 W	6	RN55C2000F	81349	
R25	Same as R14				
R26	Same as R24				
R27	Same as R14				
R28	Same as R24				
R29	Same as R14				
R30	Same as R24				
R31	Same as R14				
R32	Same as R24				
R33	Same as R14				
R34	Same as R24				
R35	Same as R4				
U1	Voltage Regulator	1	LM317H	27014	
U2	Integrated Circuit	1	MC145158P	04713	
U3	Integrated Circuit	1	LT1007CH	4W715	
U4	Integrated Circuit	1	SP8719B	52648	
U5	Integrated Circuit	1	SN74LS390N	01295	
U6	Integrated Circuit	1	CD4049AE	02735	
U7	Integrated Circuit	1	CD4081BE	04713	
Y1	Crystal 10 MHz	1	91805-41	14632	

5.5.6

TYPE 796370-1 BASEBAND AMPLIFIER

REF DESIG PREFIX A11

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	Baseband Amplifier Assembly	1	380576-1	14632	
C1	Capacitor, Ceramic, Feedthru: 330 pF, 10%, 500 V	4	54-794-001-3311	33095	
C2	Same as C1				
C3	Same as C1				
C4	Same as C1				
C5	Capacitor, Ceramic, Feedthru: 1000 pF, 500 V	3	54-794-009-102W	33095	
C6	Same as C5				
C7	Same as C5				
J1	Connector, Receptacle	7	UG1094U	80058	
J2 Thru J7	Same as J1				
J8	Connector, Receptacle	6	2012-7511-000	19505	
J9 Thru J13	Same as J8				

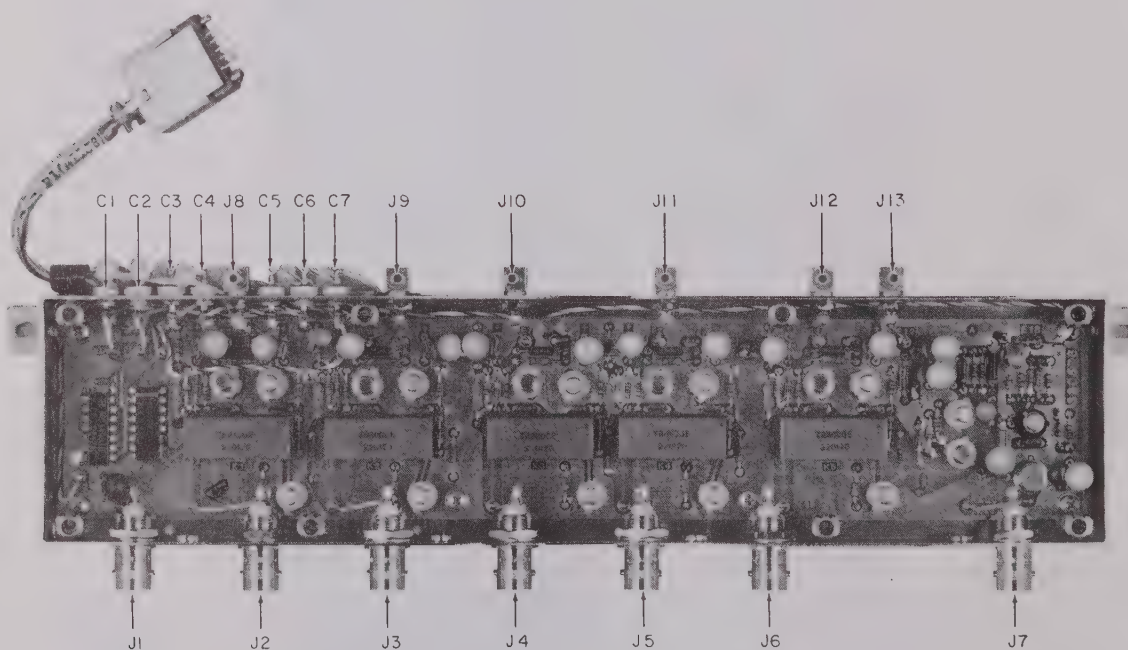


Figure 5-18. Type 796370-1 Baseband Amplifier (A11),
Location of Components

5.5.6.1 Part 380576-1 Baseband Amplifier Assembly

REF DESIG PREFIX A11A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 0.1 μ F, 20%, 50 V	7	34475-1	14632	
C2	Capacitor, Ceramic, Disc: 0.47 μ F, 20%, 50 V	6	34452-1	14632	
C3	Capacitor, Electrolytic, Tantalum: 47 μ F, 20%, 20 V	14	196D476X0020PE4	56289	
C4	Same as C3				
C5	Capacitor, Ceramic, Monolithic: 39 pF, $\pm$ 2%, 100 V, NPO	6	150-100-NPO-390G	51642	
C6	Same as C1				
C7	Same as C2				
C8	Same as C3				
C9	Same as C3				
C10	Same as C5				
C11	Same as C1				
C12	Same as C2				
C13	Same as C3				
C14	Same as C3				
C15	Same as C5				
C16	Same as C1				
C17	Same as C2				
C18	Same as C3				
C19	Same as C3				
C20	Same as C5				
C21	Same as C1				
C22	Same as C2				
C23	Same as C3				
C24	Same as C3				
C25	Same as C5				
C26	Same as C1				
C27	Same as C3				
C28	Same as C3				
C29	Same as C5				
C30	Capacitor, Electrolytic, Tantalum: 18 μ F, 10%, 20 V	3	196D186X9020KE3	56289	
C31	Same as C2				
C32	Capacitor, Ceramic, Disc: 18 pF, 5%, 50 V, NPO	1	8101-050-COGO-180J	72982	
C33	Same as C3				
C34	Same as C3				
C35	Same as C30				
C36	Same as C30				
C37	Capacitor, Electrolytic, Tantalum: 100 μ F, 10%, 10 V	1	196D107X0010PE4	56289	
C38	Same as C1				
CR1	Diode	5	IN4449	80131	

REF DESIG PREFIX A11A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR2 Thru CR5	Same as CR1				
K1	Relay, Reed	5	220-120-M	31951	
K2 Thru K5	Same as K1				
Q1	Transistor	6	U310	17856	
Q2	Transistor	6	2N3251	80131	
Q3	Transistor	5	2N2222A	80131	
Q4	Same as Q1				
Q5	Same as Q2				
Q6	Same as Q3				
Q7	Same as Q1				
Q8	Same as Q2				
Q9	Same as Q3				
Q10	Same as Q1				
Q11	Same as Q2				
Q12	Same as Q3				
Q13	Same as Q1				
Q14	Same as Q2				
Q15	Same as Q3				
Q16	Same as Q1				
Q17	Same as Q2				
Q18	Transistor	1	2N2857	80131	
R1	Resistor, Fixed, Film: 3.3 M Ω , 5%, 1/8 W	6	CF 1/8-3.3M/J	09021	
R2	Resistor, Fixed, Film: 1.0 M Ω , 5%, 1/8 W	6	CF 1/8-1M/J	09021	
R3	Resistor, Fixed, Film: 1.0 k Ω , 5%, 1/8 W	6	CF 1/8-1.0K/J	09021	
R4	Resistor, Fixed, Film: 270 Ω , 5%, 1/4 W	6	CF 1/4-270 OHMS,J	09021	
R5	Resistor, Fixed, Film: 47 Ω , 5%, 1/8 W	13	CF 1/8-47 OHMS/J	09021	
R6	Same as R5				
R7	Resistor, Fixed, Film: 47.5 Ω , 1%, 1/10 W	6	RN55C47R5F	81349	
R8	Resistor, Fixed, Film: 75 Ω , 1%, 1/10 W	5	RN55C75R0F	81349	
R9	Resistor, Fixed, Film: 56 Ω , 5%, 1/8 W	5	CF 1/8-56 OHMS/J	09021	
R10	Resistor, Fixed, Film: 15 k Ω , 5%, 1/8 W	5	CF 1/8-15K/J	09021	
R11	Same as R8				
R12	Same as R9				
R13	Same as R10				
R14	Same as R1				
R15	Same as R2				
R16	Same as R3				

REF DESIG PREFIX A11A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R17	Same as R4				
R18	Same as R5				
R19	Same as R5				
R20	Same as R7				
R21	Same as R8				
R22	Same as R9				
R23	Same as R10				
R24	Same as R1				
R25	Same as R2				
R26	Same as R3				
R27	Same as R4				
R28	Same as R5				
R29	Same as R5				
R30	Same as R7				
R31	Same as R8				
R32	Same as R9				
R33	Same as R10				
R34	Same as R1				
R35	Same as R2				
R36	Same as R3				
R37	Same as R4				
R38	Same as R5				
R39	Same as R5				
R40	Same as R7				
R41	Same as R8				
R42	Same as R9				
R43	Same as R10				
R44	Same as R1				
R45	Same as R2				
R46	Same as R3				
R47	Same as R4				
R48	Same as R5				
R49	Same as R5				
R50	Same as R7				
R51	Same as R1				
R52	Same as R2				
R53	Same as R3				
R54	Same as R4				
R55	Same as R5				
R56	Same as R5				
R57	Same as R7				

REF DESIG PREFIX A11A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R58	Resistor, Fixed, Film: 82.5 Ω , 1%, 1/10 W	1	RN55C82R5F	81349	
R59	Resistor, Fixed, Film: 33 Ω , 5%, 1/8 W	1	CF 1/8-33 OHMS/J	09021	
R60	Resistor, Fixed, Film: 13 k Ω , 5%, 1/8 W	1	CF 1/8-13K/J	09021	
R61	Resistor, Fixed, Film: 4.7 k Ω , 5%, 1/8 W	1	CF 1/8-4.7K/J	09021	
R62	Resistor, Fixed, Film: 475 Ω , 1%, 1/10 W	1	RN55C4750F	81349	
R63	Resistor, Fixed, Film: 221 Ω , 1%, 1/10 W	1	RN55C2210F	81349	
R64	Resistor, Fixed, Film: 39 k Ω , 5%, 1/8 W	1	CF 1/8-39K/J	09021	
R65	Same as R5				
R66	Resistor, Fixed, Film: 100 Ω , 5%, 1/8 W	1	CF 1/8-100 OHMS/J	09021	
R67	Resistor, Fixed, Film: 68.1 Ω , 1%, 1/10 W	1	RN55C68R1F	81349	
U1	Integrated Circuit	1	CD4094BE	02735	
U2	Integrated Circuit	1	LH0002CH	27014	
U3	Integrated Circuit	1	MC14081BCD	04713	

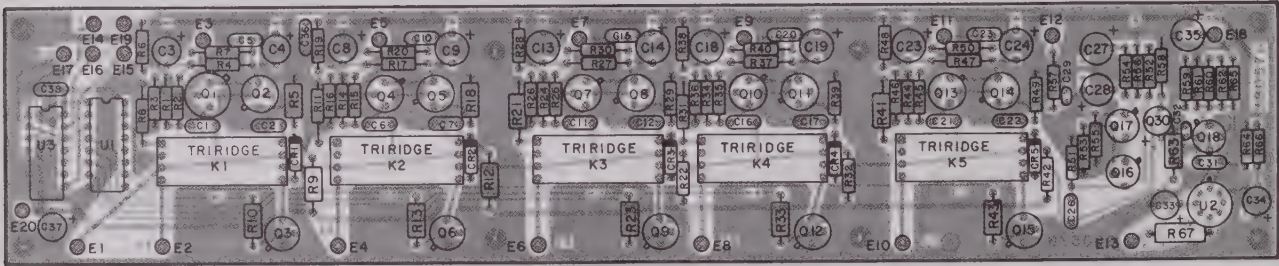


Figure 5-19. Part 380576-1 Baseband Amplifier Assembly (A11A1),
Location of Components

5.5.7 TYPE 796376-1 REFERENCE GENERATOR

REF DESIG PREFIX A12

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	Reference Generator Assembly	1	380580-1	14632	
C1	Capacitor, Ceramic, Feedthru: 1000 pF, 500 V	3	54-794-009-102W	33095	
C2	Same as C1				
C3	Same as C1				
J1	Connector, Receptacle	1	UG1094U	80058	
J2	Connector, Receptacle	7	2012-7511-000	19505	
J3 Thru J8	Same as J2				
U1	OSC, Ovenized	1	841046	14632	

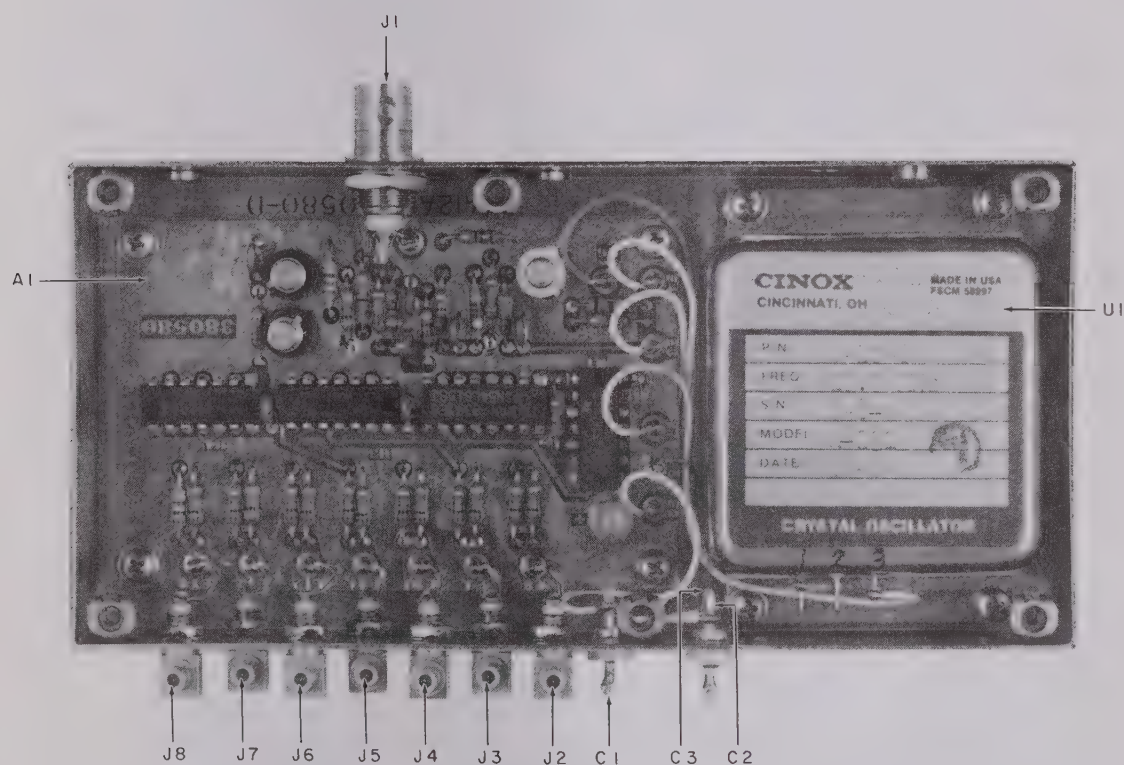


Figure 5-20. Type 796376-1 Reference Generator (A12),
Location of Components

5.5.7.1 Part 380580-1 Reference Generator Assembly

REF DESIG PREFIX A12A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Electrolytic, Tantalum: 100 μ F, 10%, 10 V	1	196D107X0010PE4	56289	
C2	Capacitor, Ceramic, Disc: 0.1 μ F, 20%, 50 V	10	34475-1	14632	
C3					
Thru	Same as C2				
C11					
E1	Terminal, Forked	14	140-1941-02-01	71279	
E2					
Thru	Same as E1				
E13					
L1	Coil, Fixed, Mold: 1.0 μ H, 10%	1	1025-20 (75083-13)	99800	
L2	Coil, Fixed, Mold: 220 μ H, 10%	1	1025-76 (75085-11)	99800	
Q1	Transistor	2	2N2857	80131	
Q2	Same as Q1				
Q3	Transistor	1	2N2222A	80131	
R1	Resistor, Fixed, Film: 56 Ω , 5%, 1/4 W	1	CF 1/4-56 OHMS/J	09021	
R2	Resistor, Fixed, Film: 12 k Ω , 5%, 1/4 W	1	CF 1/4-12K/J	09021	
R3	Resistor, Fixed, Film: 4.7 k Ω , 5%, 1/4 W	1	CF 1/4-4.7K/J	09021	
R4	Resistor, Fixed, Film: 47 Ω , 5%, 1/4 W	2	CF 1/4-47 OHMS/J	09021	
R5	Resistor, Fixed, Film: 1.0 k Ω , 5%, 1/4 W	1	CF 1/4-1K/J	09021	
R6	Resistor, Fixed, Film: 220 Ω , 5%, 1/4 W	1	CF 1/4-220 OHMS/J	09021	
R7	Resistor, Fixed, Film: 18 k Ω , 5%, 1/4 W	1	CF 1/4-18K/J	09021	
R8	Same as R4				
R9	Resistor, Fixed, Film: 680 Ω , 5%, 1/4 W	1	CF 1/4-680 OHMS/J	09021	
R10	Resistor, Fixed, Film: 22 k Ω , 5%, 1/4 W	2	CF 1/4-22K/J	09021	
R11	Same as R10				
R12	Resistor, Fixed, Film: 2.2 k Ω , 5%, 1/4 W	2	CF 1/4-2.2K/J	09021	
R13	Same as R12				
R14	Resistor, Fixed, Film: 100 Ω , 5%, 1/4 W	7	CF 1/4-100 OHMS/J	09021	
R15	Resistor, Fixed, Film: 10 k Ω , 5%, 1/4 W	7	CF1/4-10K/J	09021	
R16	Same as R14				
R17	Same as R15				
R18	Same as R14				
R19	Same as R15				
R20	Same as R14				
R21	Same as R15				
R22	Same as R14				
R23	Same as R15				
R24	Same as R14				
R25	Same as R15				
R26	Same as R14				
R27	Same as R15				
U1	Integrated Circuit	1	SN74LS290N	01295	
U2	Integrated Circuit	1	SN74LS158N	01295	
U3	Integrated Circuit	2	SN74LS04N	01295	
U4	Same as U3				

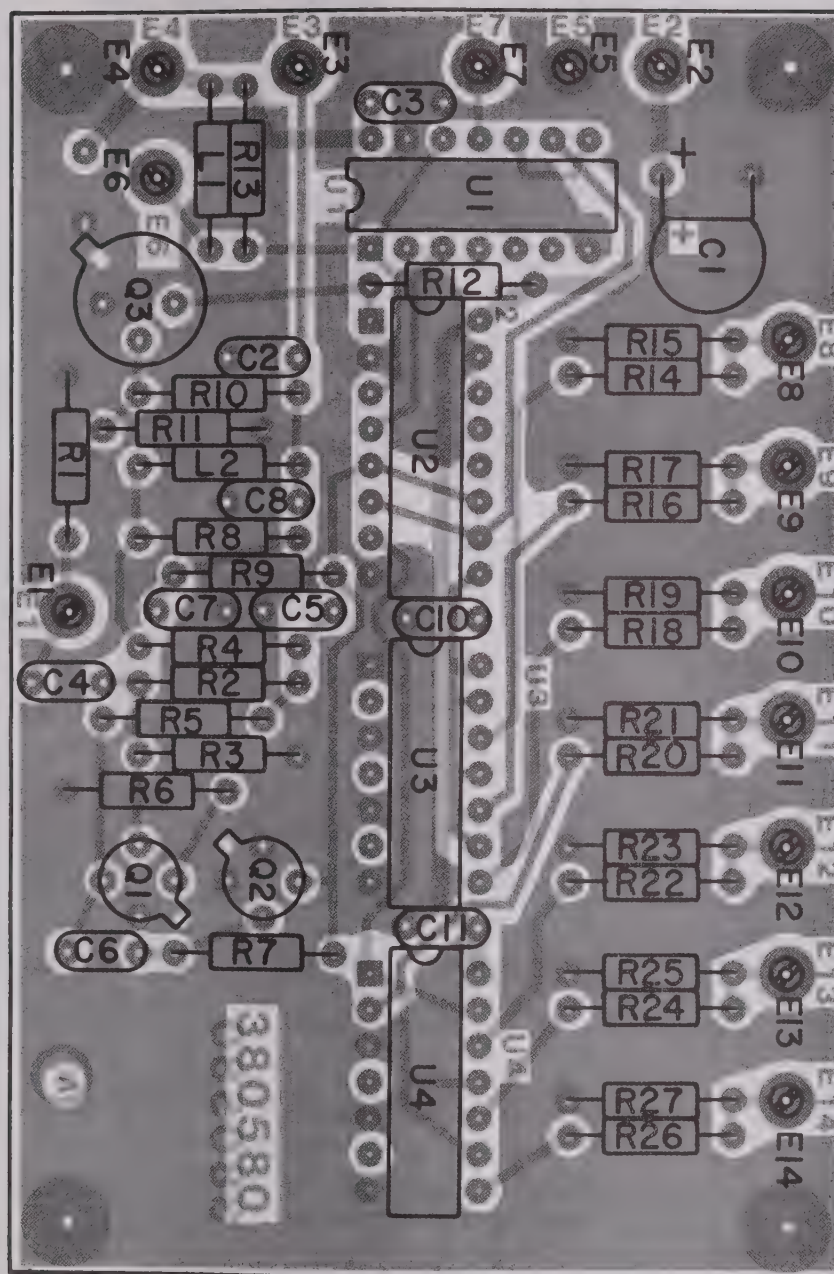


Figure 5-21. Part 380580-1 Reference Generator Assembly (A12A1),
Location of Components

5.5.8 TYPE 796380-1, KEYBOARD

REF DESIG PREFIX A13

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
J1	Connector, Receptacle	1	609-2007	22526	
MP1	Spacer Board PC Assembly	1	796388-1	14632	
S1	Switch Button Engraved	1	380594-13	14632	
S2	Switch Button Engraved	1	380594-14	14632	
S3	Switch Button Engraved	1	380594-15	14632	
S4	Switch Button Engraved	1	380594-7	14632	
S5	Switch Button Engraved	1	380594-8	14632	
S6	Switch/Marked	1	380594-9	14632	
S7	Switch/Marked	1	380594-2	14632	
S8	Switch/Marked	1	380594-3	14632	
S9	Switch/Marked	1	380594-4	14632	
S10	Switch/Marked	1	380594-19	14632	
S11	Switch/Marked	1	380594-6	14632	
S12	Switch/Marked	1	380594-11	14632	
S13	Switch/Marked	1	380594-17	14632	
S14	Switch/Marked	1	380594-23	14632	
S15	Switch/Marked	1	380594-29	14632	
S16	Switch/Marked	1	380594-5	14632	
S17	Switch/Marked	1	380594-10	14632	
S18	Switch/Marked	1	380594-16	14632	
S19	Switch/Marked	1	380594-30	14632	
S20	Switch/Marked	1	380594-12	14632	
S21	Switch/Marked	1	380594-18	14632	
S22	Switch/Marked	1	380594-24	14632	
S23	Switch/Marked	1	380594-20	14632	
S24	Switch/Marked	1	380594-21	14632	
S25	Switch/Marked	1	380594-22	14632	
S26	Switch/Marked	1	380594-27	14632	
S27	Switch/Marked	1	380594-28	14632	
S28	Switch/Marked	1	380594-26	14632	
S29	Switch/Marked	1	380594-1	14632	
S30	Switch/Marked	1	380594-25	14632	

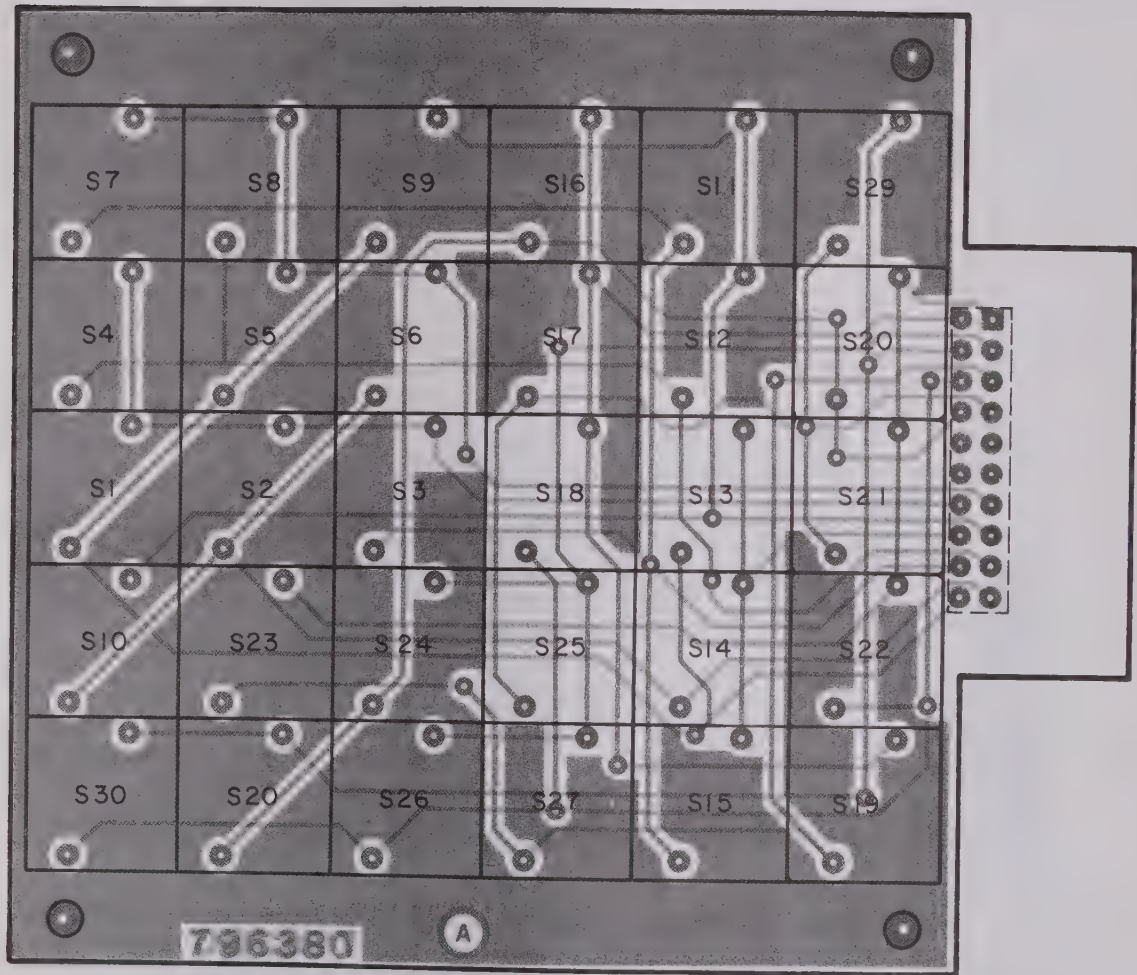


Figure 5-22. Type 796380-1 Keyboard (A13),
Location of Components

5.5.9 TYPE 766013-1 POWER SUPPLY		REF DESIG PREFIX A14			
REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	Power Supply Assembly No. 1	1	380653-1	14632	
A2	Power Supply Assembly No. 2	1	380668-1	14632	
Q1	Transistor	1	2N4398	80131	
U1	Voltage Regulator	1	LM338K	27014	
U2	Voltage Regulator	1	LM337K	27014	

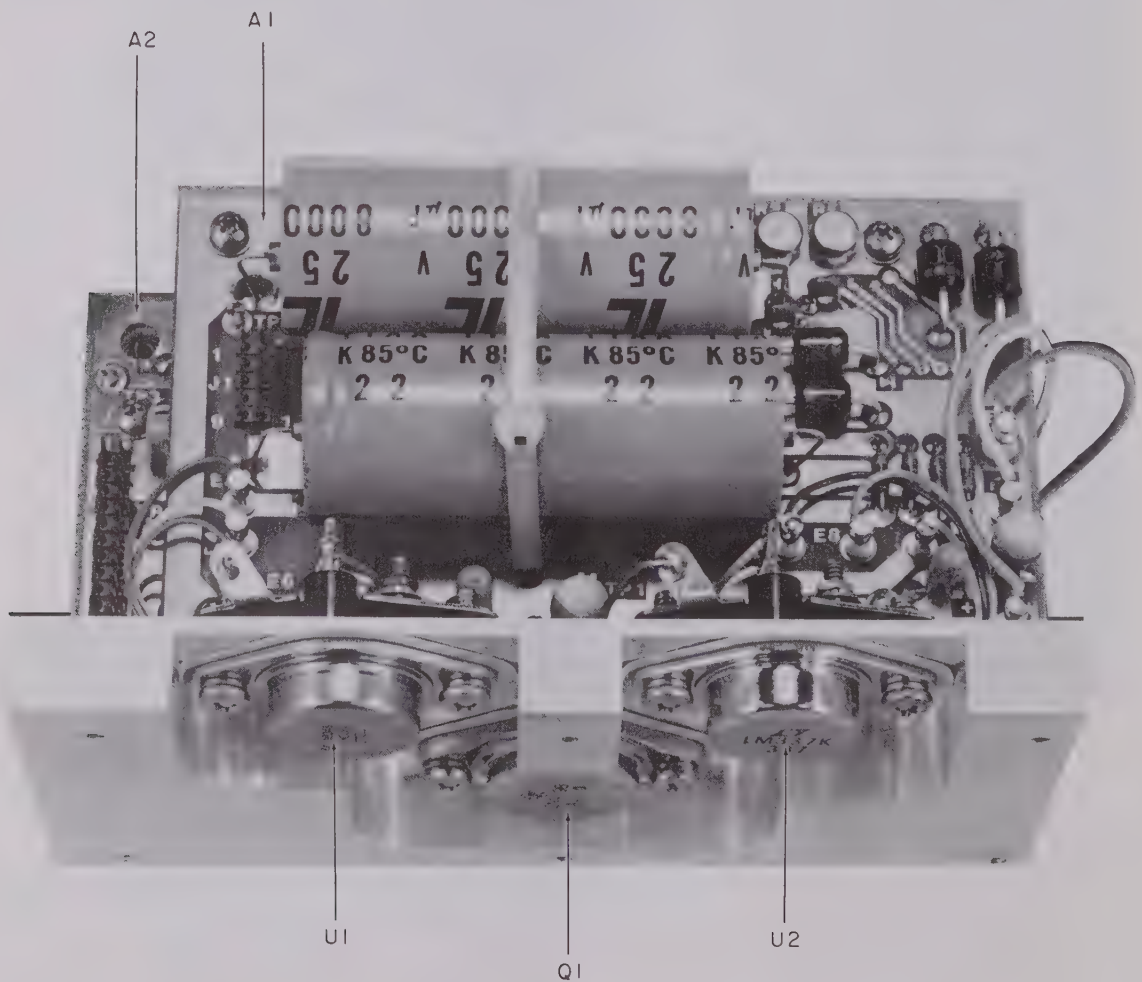


Figure 5-23. Type 766013-1 Power Supply (A14),
Location of Components

5.5.9.1 Part 380653-1 Power Supply Assy. No. 1

REF DESIG PREFIX A14A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Electrolytic, Aluminum: 8000 μ F, 10%, 25 V	2	808TTA025A	74840	
C2	Same as C1				
C3	Capacitor, Ceramic, Disc: 0.1 μ F, 20%, 50 V	2	34475-1	14632	
C4	Same as C3				
C5	Capacitor, Electrolytic, Tantalum: 10 μ F, 20%, 20 V	2	196D106X0020JE3	56289	
C6	Same as C5				
C7	Capacitor, Electrolytic, Tantalum: 47 μ F, 20%, 20 V	2	196D476X0020PE4	56289	
C8	Same as C7				
E1	Terminal, Turret	9	160-2034-02-01	71279	
E2 Thru E8	Same as E1				
J1	Header Assembly	1	65610-110	22526	
R1	Resistor, Fixed, Film: 121 Ω , 1%, 1/10 W	2	RN55C1210F	81349	
R2	Resistor, Variable, Film: 200 Ω , 10%, 1/2 W	2	62PAR200	73138	
R3	Resistor, Fixed, Film: 1.21 k Ω , 1%, 1/2 W	2	RN55C1211F	81349	
R4	Same as R1				
R5	Same as R2				
R6	Same as R3				
TP1	Terminal, Forked	2	140-1941-02-01	71279	
TP2	Same as TP1				

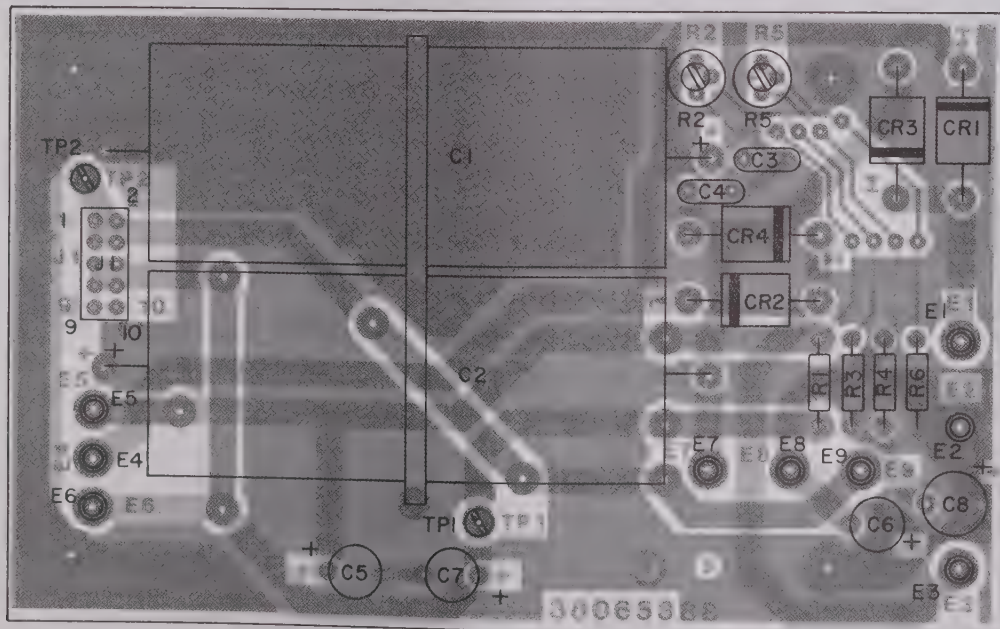


Figure 5-24. Part 380653-1 Power Supply Assembly No. 1 (A14A1),
Location of Components

5.5.9.2 Part 380668-1 Power Supply Assy. No. 2

REF DESIG PREFIX A14A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Electrolytic, Aluminum: 33,000 μ F, 10% + 50%, 10 V	1	339TTA010A	74840	
C2	Capacitor, Electrolytic, Tantalum: 4.7 μ F, 20%, 35 V	2	196D475X0035JE3	56289	
C3	Capacitor, Ceramic, Disc: 0.047 μ F, 10%, 100 V	1	CK06BX473K	81349	
C4	Capacitor, Ceramic, Disc: 0.47 μ F, 20%, 50 V	1	34452-1	14632	
C5	Capacitor, Electrolytic, Tantalum: 10 μ F, 20%, 20 V	1	196D106X0020JE3	56289	
C6	Capacitor, Ceramic, Disc: 0.22 μ F, 10%, 50 V	1	8131-050-X7R0-224K	72982	
C7	Capacitor, Ceramic, Disc: 0.1 μ F, 20%, 50 V	1	34475-1	14632	
C8	Same as C2				
C9	Capacitor/Electrolytic, Tantalum: 18 μ F, 10%, 20 V	2	196D186X9020KE3	56289	
C10	Same as C9				
C11	Capacitor, Electrolytic, Tantalum: 47 μ F, 20%, 20 V	1	196D76XX0020PE4	56289	
CR1	Diode	1	LVA 56A	01281	
E1	Terminal, Turret	6	160-2034-02-01	71279	
E2 Thru E5	Same as E1				
J1	24 Pin Header	1	65610-124	22526	
L1	Coil, Fixed: 4.7 mH, 10%	1	553-3635-45	71279	
L2	Inductor, Fixed	1	1131-109	14632	
R1	Not Used				
R2	Resistor, Fixed, Film: 2.0 k Ω , 1%, 1/10 W	1	RN55C2001F	81349	
R3	Resistor, Fixed, Film: 1.0 k Ω , 1%, 1/10 W	1	RN55C1001F	81349	
R4	Resistor, Fixed, Composition: 33 Ω , 5%, 1/4 W	1	RCR07G330JS	81349	
R5	Resistor, Fixed, Film: 680 Ω , 5%, 1/4 W	1	CF 1/4-680 OHMS/J	09021	
R6	Resistor, Fixed, Film: 511 Ω , 1%, 1/10 W	1	RN55C5110F	81349	
R7	Resistor, Fixed, Film: 1.21 k Ω , 1%, 1/10 W	1	RN55C1211F	81349	
TP1	Terminal Forked	3	140-1941-02-01	71279	
TP2	Same as TP1				
TP3	Same as TP1				
U1	Diode	1	ESAC82-004		
U2	Integrated Circuit	1	UC2834N	12969	
U3	Converter	1	EM 671	62506	

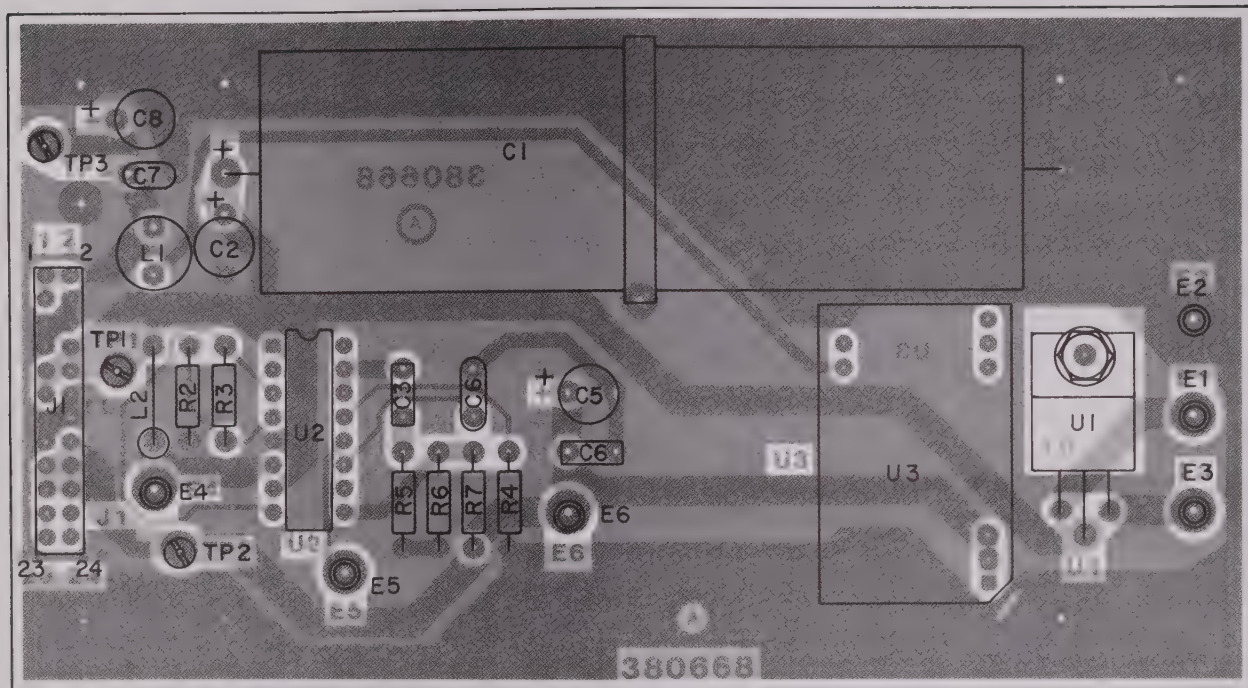


Figure 5-25. Part 380668-1 Power Supply Assembly No. 2 (A14A2),
Location of Components

SECTION VI
SCHEMATICS

NOTES
UNLESS OTHERWISE SPECIFIED
CAPACITANCE IS IN μ F
RESISTANCE IS IN OHMS $\pm 5\%$ 1/4W
SMALL DIODES ARE 1N4148

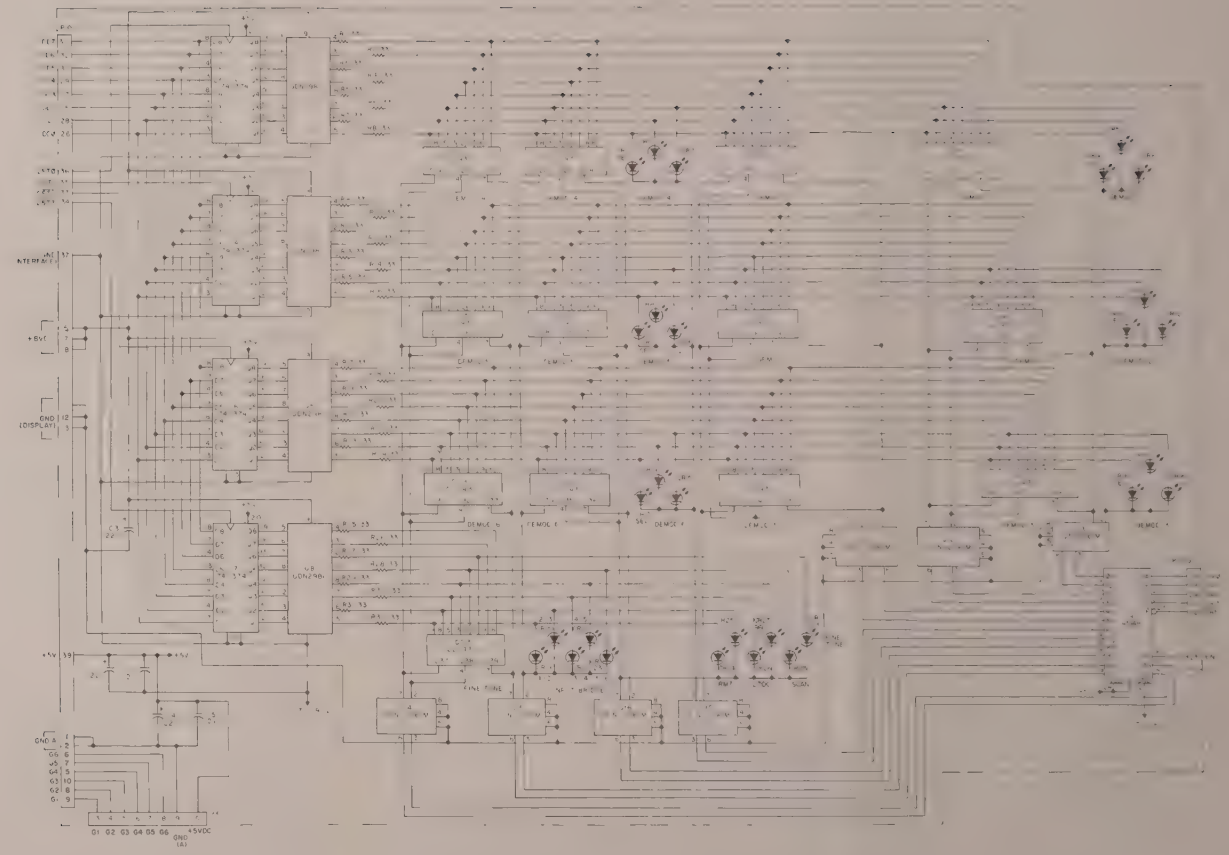


Figure 6-1. Type 796374-1, Display (A1),
Schematic Diagram 580273

NOTES:

I. UNLESS OTHERWISE SPECIFIED:

a). CAPACITANCE IS IN μF .

b). RESISTANCE IS IN OHMS, 5%, 1/4W.

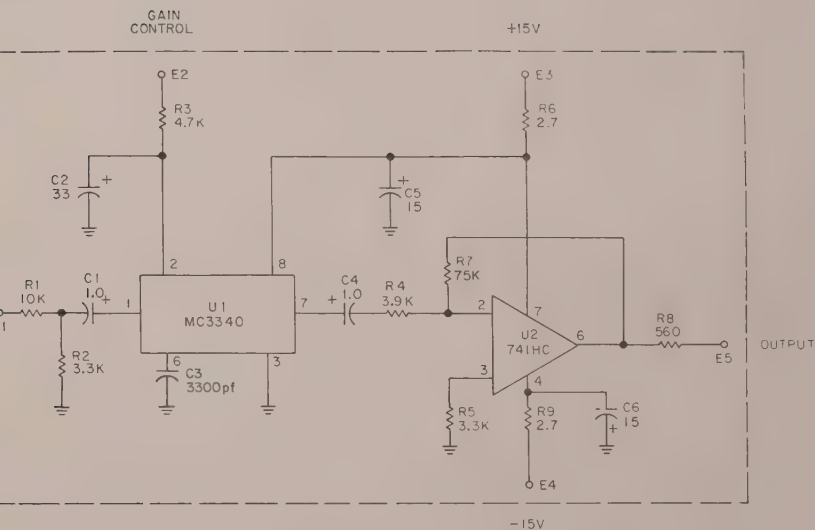


Figure 6-2. Type 796387-1, Headphone Amplifier (A2), Schematic Diagram 380651

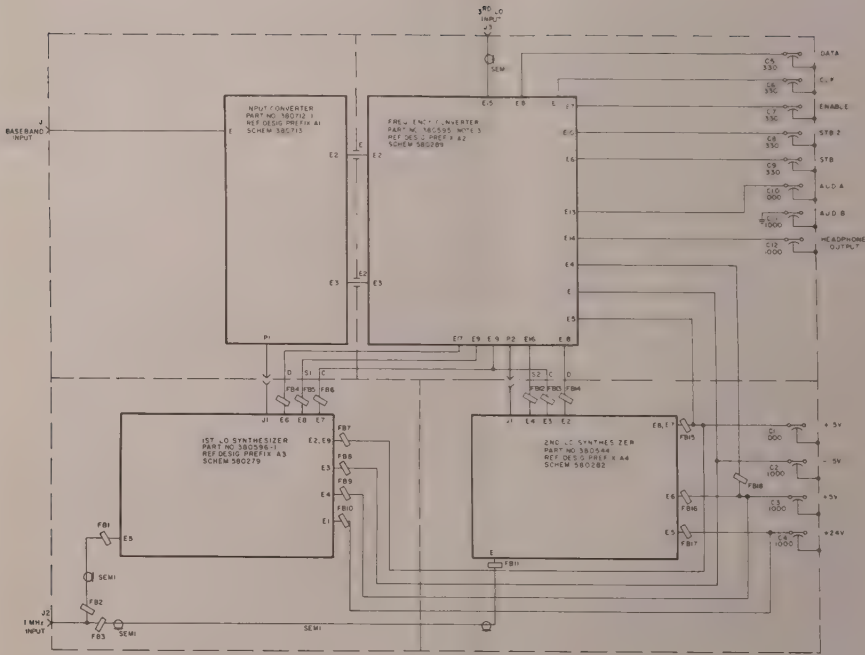
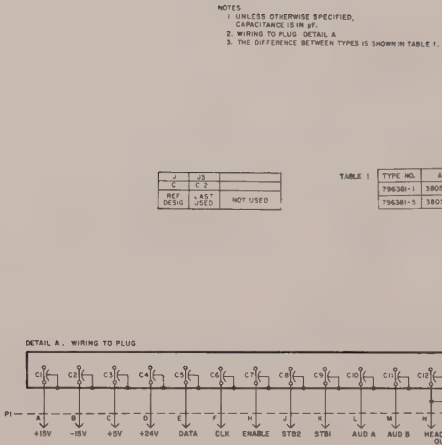


Figure 6-3. Type 796381-1, Demodulator (A3-A8), Schematic Diagram 580298

NOTES:
 1. UNLESS OTHERWISE SPECIFIED:
 a) CAPACITANCE IS IN pF.
 b) INDUCTANCE IS IN μ H.
 c) RESISTANCE IS IN OHMS, $\pm 1\%$, 1/10W

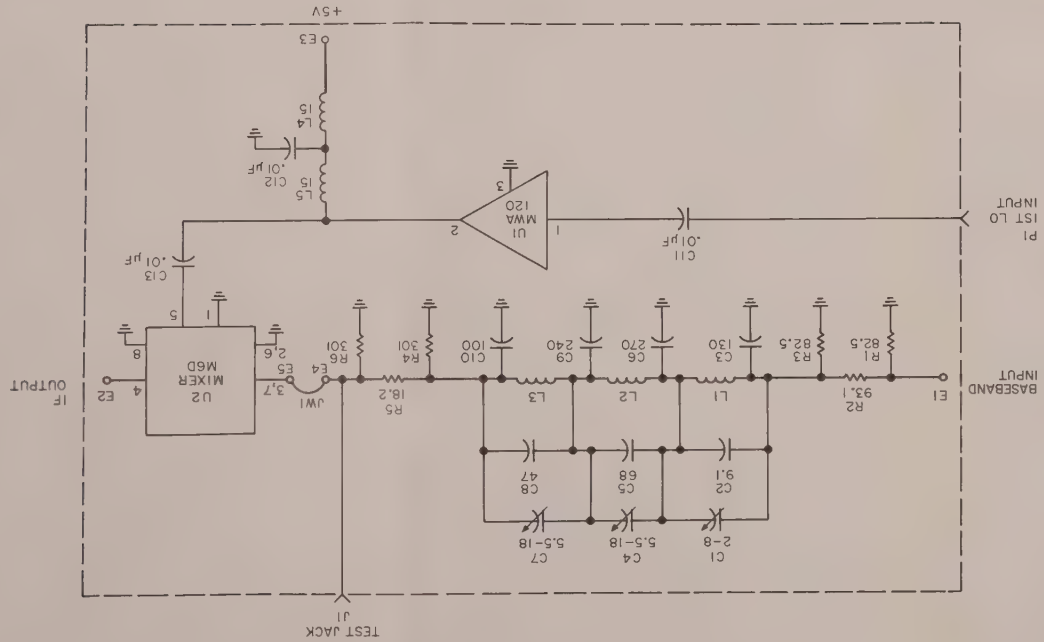


Figure 6-4. Part 380712-1, Input Converter (A3A1-A8A1),

Schematic Diagram 380713

NOTES:
 1. UNLESS OTHERWISE SPECIFIED:
 a) RESISTANCE IS IN OHMS, 5%./MM.
 b) CAPACITANCE IS IN μ F.
 2. FILS & U11 ARE PURCHASED AS A MATCHED SET.
 3. DIFFERENCE IN TYPES SHOWN IN TABLE I.

TABLE I		
TYP. NO.	FIL 2	U
380595-1	526-B476-Q20A	526-B476-Q20B
380595-2	526-B491-Q20A	526-B491-Q20B

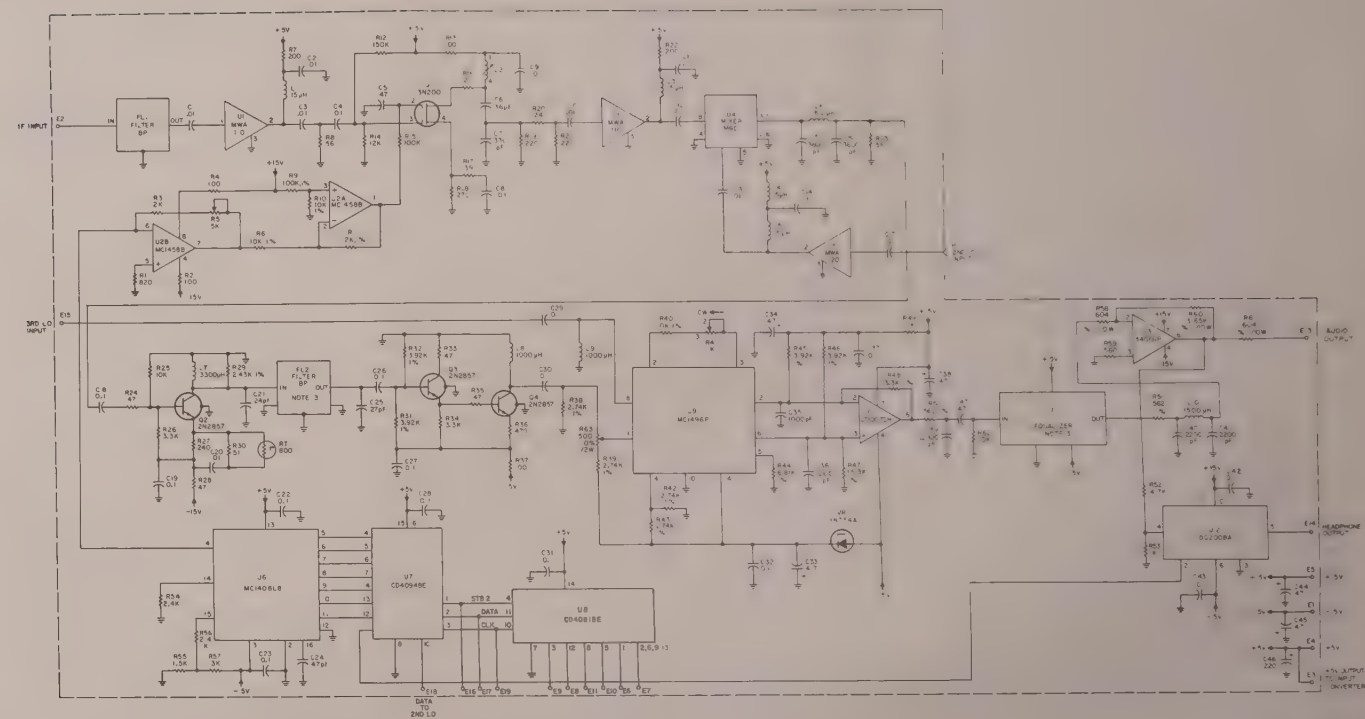


Figure 6-5. Part 380595-1, Frequency Converter (A3A2-A8A2), Schematic Diagram 580289

NOTES
 1. UNLESS OTHERWISE SPECIFIED
 a) CAPACITANCE IS IN pF.
 b) INDUCTANCE IS IN μ H.
 c) RESISTANCE IS IN OHMS, 2% 1/10W.
 d) ALL DIVIDERS ARE RY390.

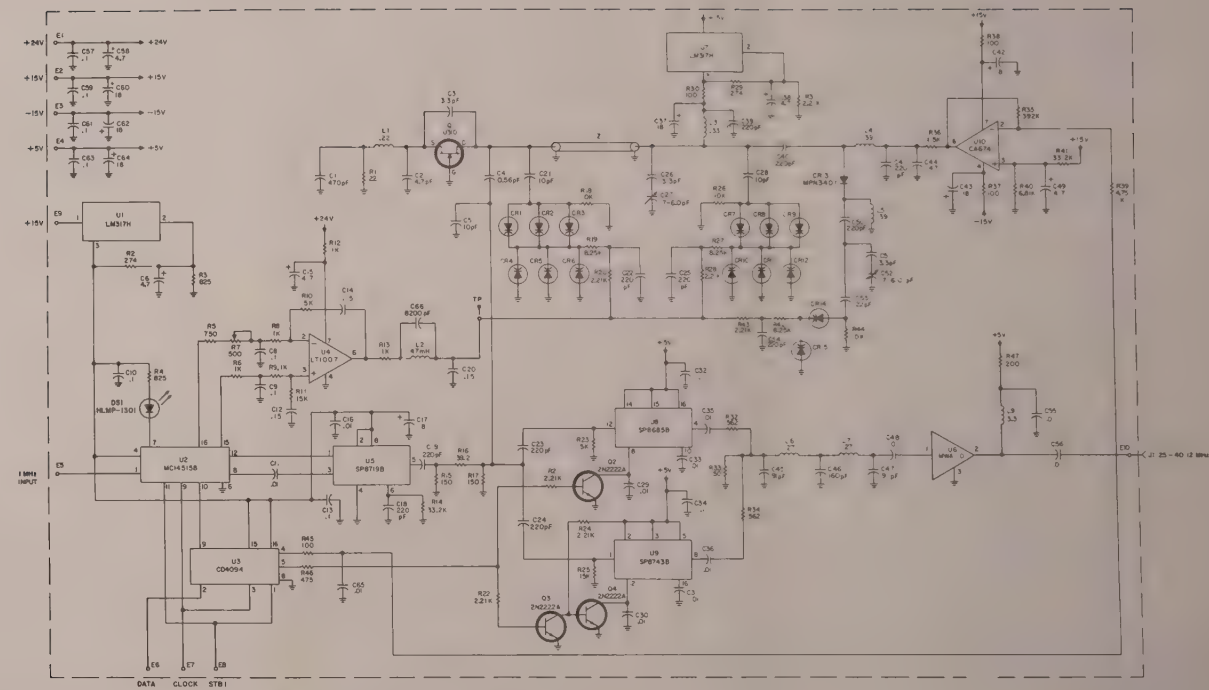


Figure 6-6. Part 380596-1, 1st LO Synthesizer (A3A3-A3A8), Schematic Diagram 580279

NOTES:
 1. UNLESS OTHERWISE SPECIFIED:
 R1 RESISTANCE IS IN OHMS, 1% TOL.
 R2 CAPACITANCE IS IN pF.
 C1 INDUCTANCE IS IN nH.
 ALL DIODES ARE KY3901.

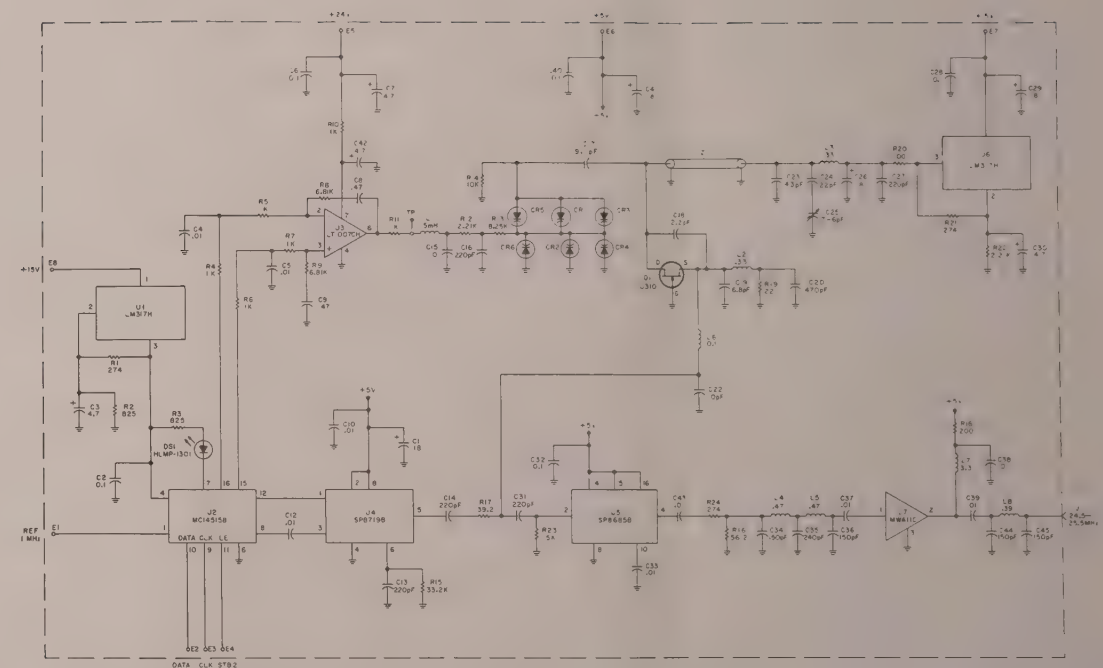
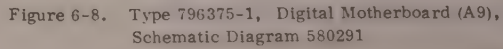


Figure 6-7. Part 380544-1, 2nd LO Synthesizer (A3A4-A8A4),
 Schematic Diagram 580282



NOTES:
 1. UNLESS OTHERWISE SPECIFIED
 ALL CAPACITANCE IS IN PF.
 ALL RESISTANCE IS IN OHMS, 5%, 1/8W.

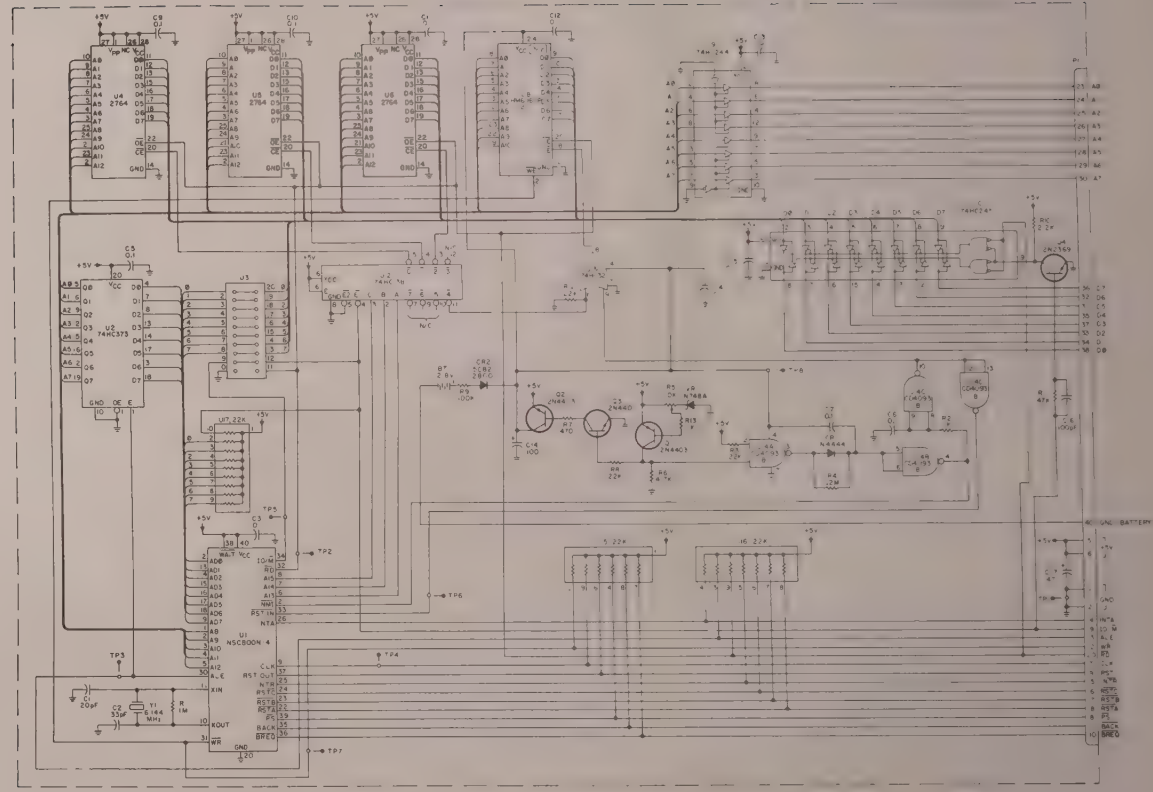
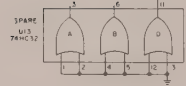
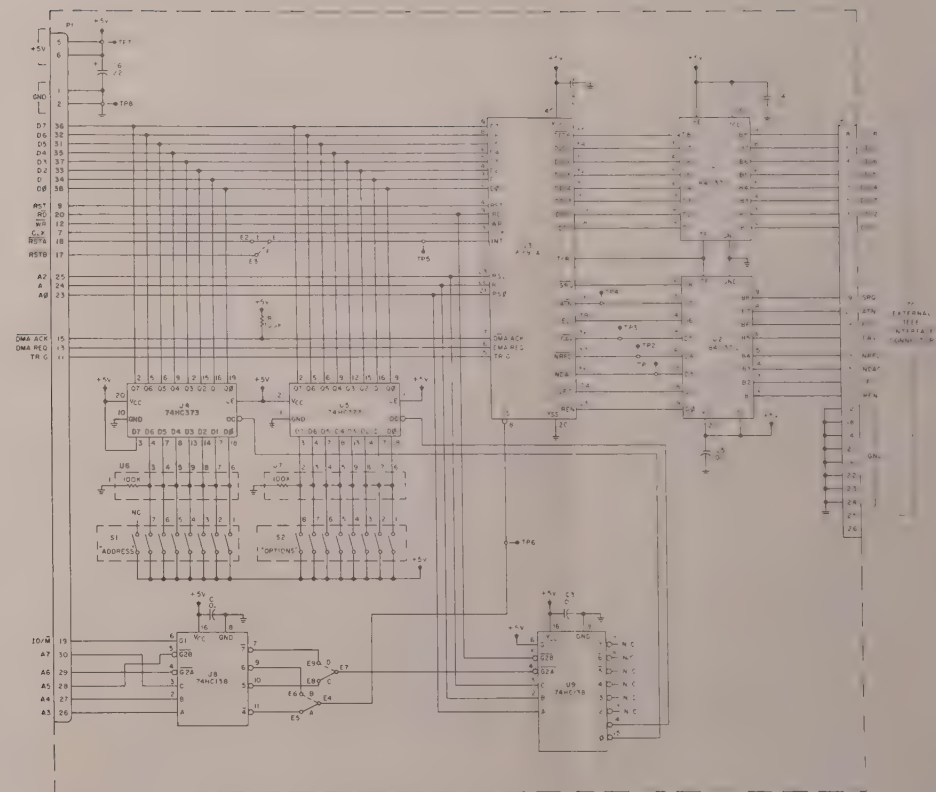


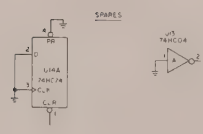
Figure 6-9. Type 796371-1, Microprocessor (A9A1),
 Schematic Diagram 580288

NOTES:
 1. UNLESS OTHERWISE SPECIFIED:
 a) RESISTANCE IS IN OHMS, 25°C, 100%
 b) CAPACITANCE IS IN pF.
 2. FOR WJ 95-88E-9S, CONNECTION HAS TO
 BE MADE FROM E1 TO E2, E4 TO E2,
 E7 TO E8

REF	HIGHEST	USED	NOT USED
1	1		
2	2		
3	3		
4	4		
5	5		
6	6		
7	7		
8	8		
9	9		
10	10		
11	11		
12	12		
13	13		
14	14		
15	15		
16	16		
17	17		
18	18		
19	19		
20	20		
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89	89		
90	90		
91	91		
92	92		
93	93		
94	94		
95	95		
96	96		
97	97		
98	98		
99	99		
100	100		



NOTE 1
UNLESS OTHERWISE SPECIFIED
ALL CAPACITANCES ARE IN PF.
RESISTANCE IS IN OHMS, %/100.
ALL IN RESISTORS ARE 100W.



Q1	Q2	
R	R1	
C1	C2	C4
REF	AST	NOT
20	100	100
SEC	SEC	SEC

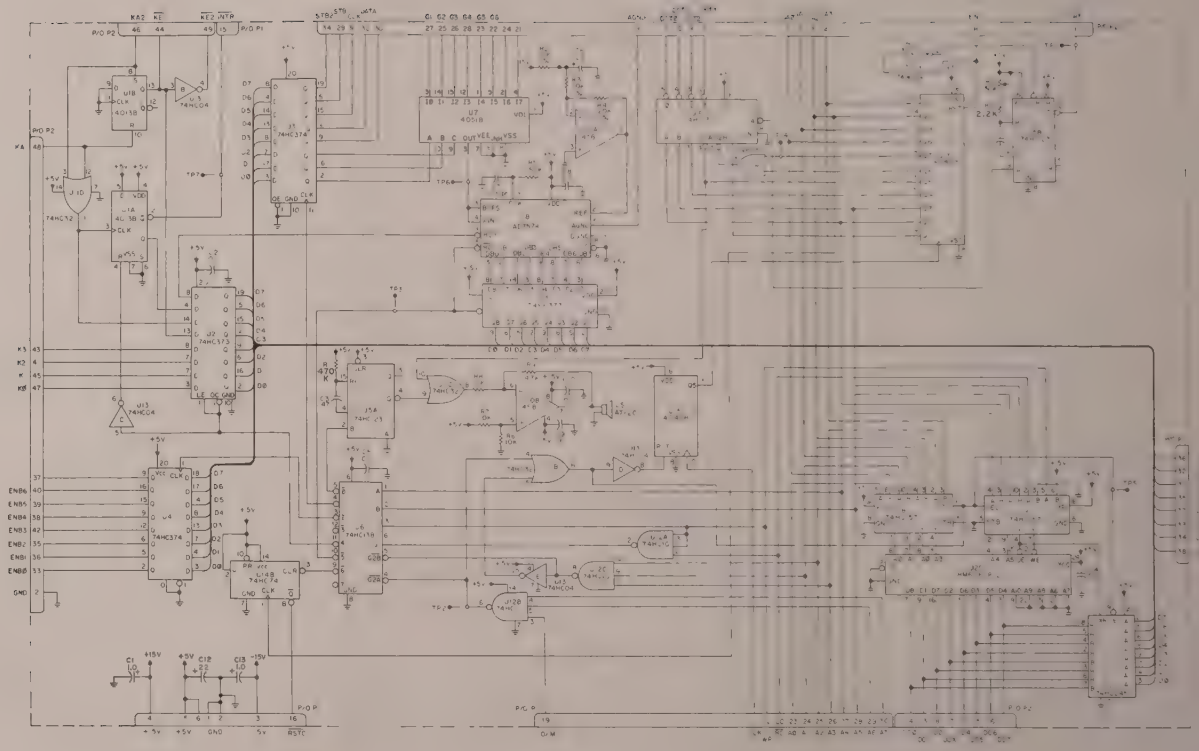


Figure 6-11. Type 796372-1 Interface (A9A3), Schematic Diagram 580275

NOTES:
1. UNLESS OTHERWISE SPECIFIED
CAPACITANCE IS IN P.F.
INDUCTANCE IS IN μ H.
RESISTANCE IS IN OHMS, 1% 1/10W.
2. OPTIMUM VALUE OF CR1 TO BE FACTORY
SELECTED.



Y	Y1
L	Q17
R	Q15
D	Q3
V	
E	E18
DS	DS
CR	CR4
L	CR4
REF	REF
DESIG	DESIG

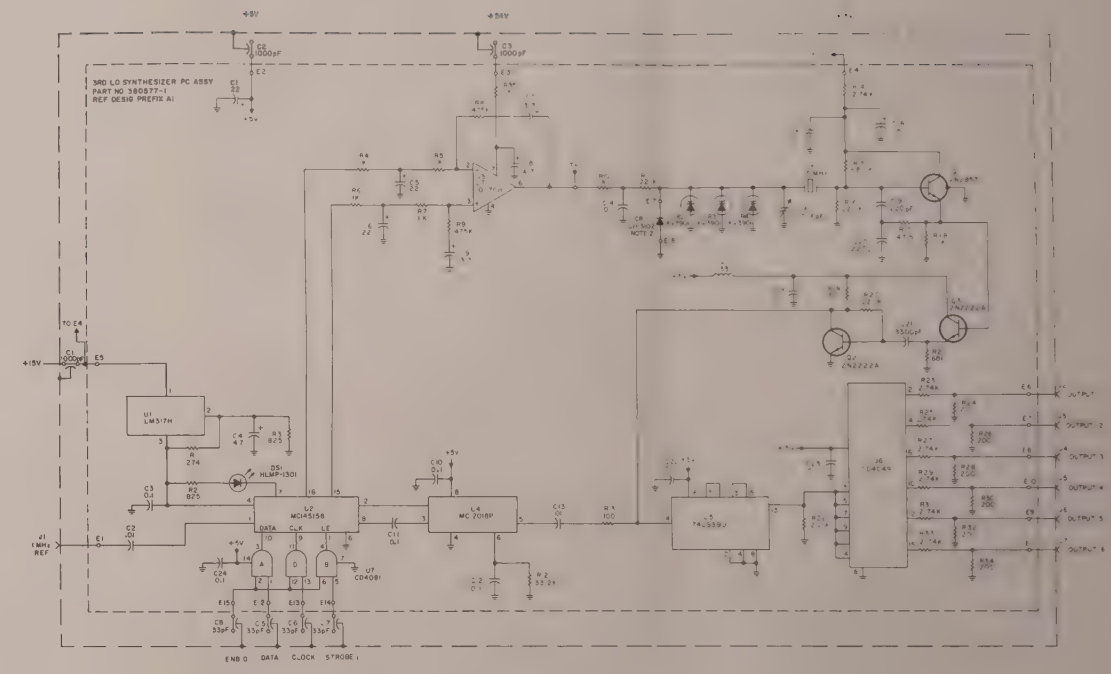
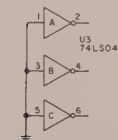


Figure 6-12. Type 776009-1, 3rd LO Synthesizer (A10), Schematic Diagram 580271

Figure 6-13. Type 796370-1, Baseband Amplifier (A11), Schematic Diagram 580272

NOTES:
 1. UNLESS OTHERWISE INDICATED,
 CAPACITANCE IS IN μ F.
 2. RESISTANCE IS IN OHMS, 5%, 1/4W.
 3. INDUCTANCE IS IN μ H.

SPARES



SPARES

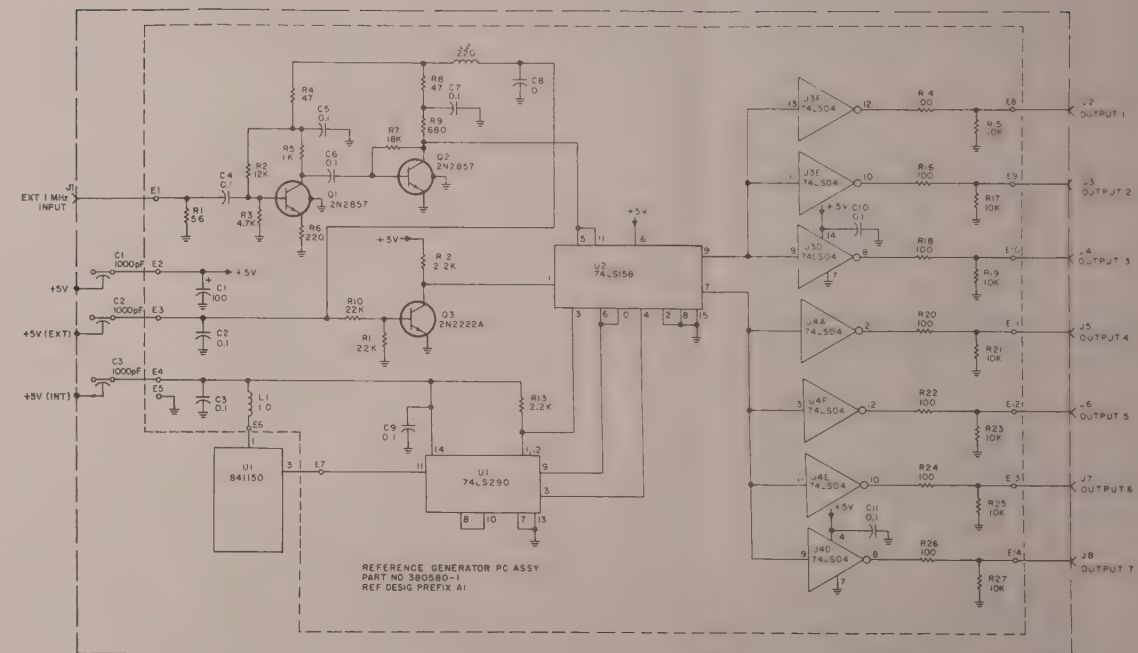
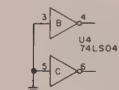


Figure 6-14. Type 796376-1, Reference Generator (A12), Schematic Diagram 480557

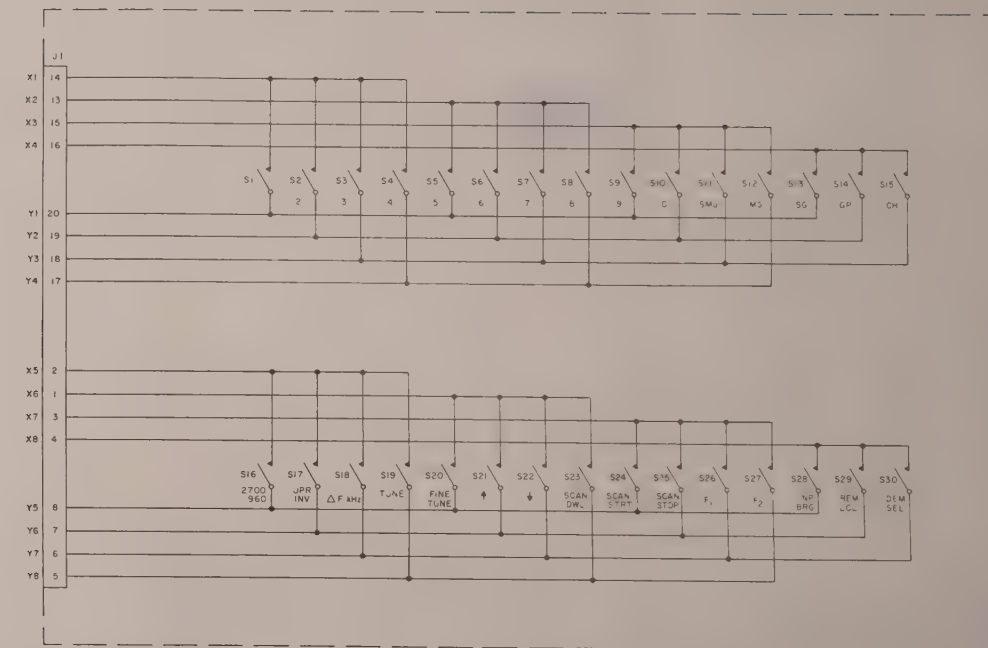


Figure 6-15. Type 796380-1, Keyboard (A13),
Schematic Diagram 480559



Figure 6-16. Type 766013-1, Power Supply (A14), Schematic Diagram 580302-1

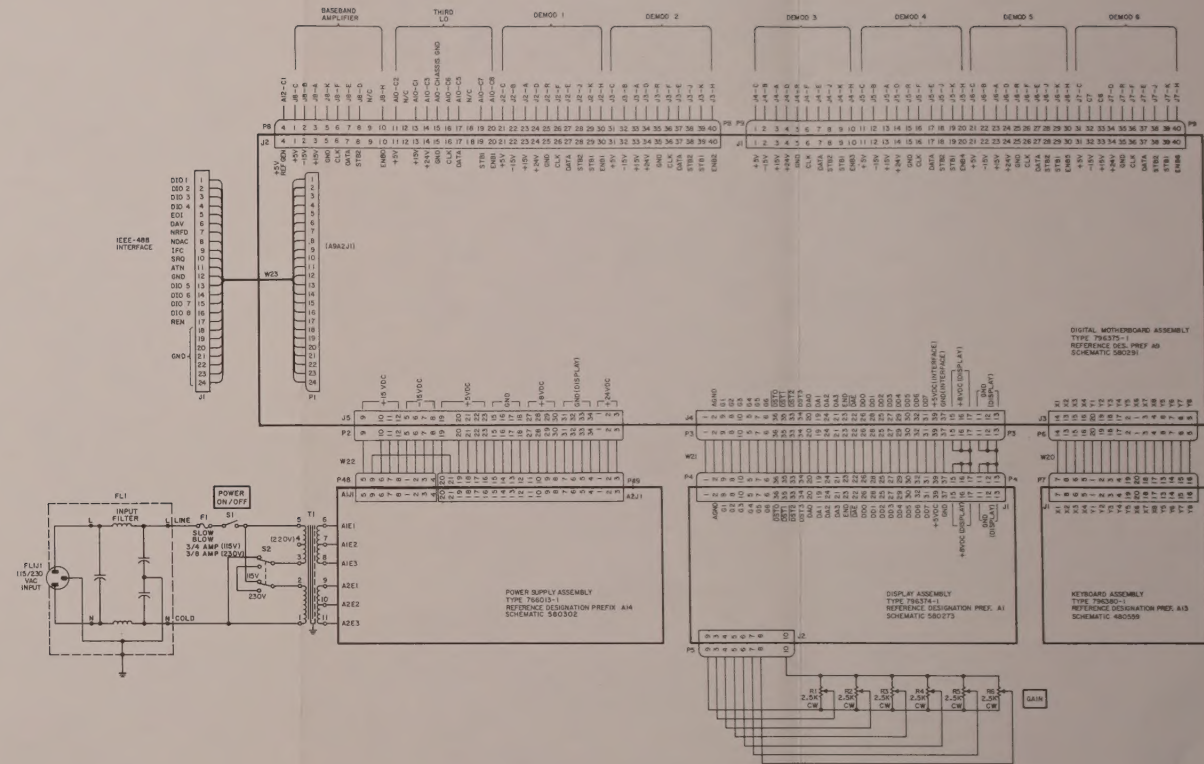
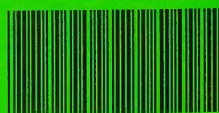


Figure 6-17. Type WJ-9518BE-9S FDM Demodulator, Main Chassis Schematic Diagram 580299 (Sheet 2 of 2)

MP MASTER



MA27809